Freescale Semiconductor
Technical Data
An Energy Efficient Solution by Freescale

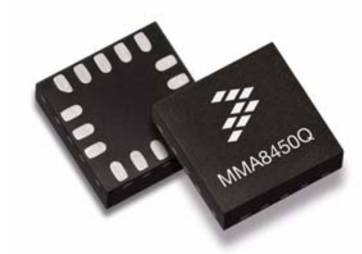
MMA8450Q
Rev 5, 04/2010
RoHS

3-Axis, 8-bit/12-bit Digital Accelerometer

MMA8450Q

MMA8450Q: XYZ-AXIS ACCELEROMETER ±2g/±4g/±8g

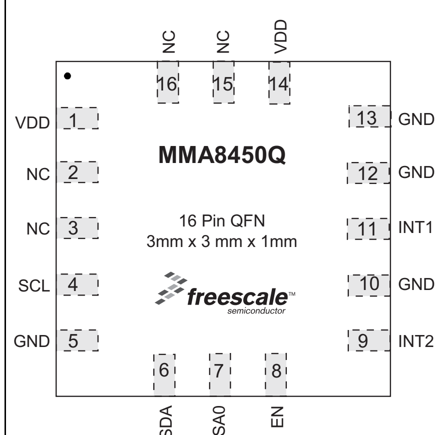
Top and Bottom View



16 PIN QFN
CASE 2077-01

The MMA8450Q is a smart low-power, three-axis, capacitive micromachined accelerometer featuring 12 bits of resolution. This accelerometer is packed with embedded functions with flexible user programmable options, configurable to two interrupt pins. Embedded interrupt functions allow for overall power savings relieving the host processor from continuously polling data. The MMA8450Q's Embedded FIFO buffer can be configured to log up to 32 samples of X,Y and Z-axis 12-bit (or 8-bit for faster download) data. The FIFO enables a more efficient analysis of gestures and user programmable algorithms, ensuring no loss of data on a shared I^{2}C bus, and enables system level power saving (up to 96% of the total power consumption savings) by allowing the applications processor to sleep while data is logged. There is access to both low pass filtered data as well as high pass filtered data, which minimizes the data analysis required for jolt detection and faster transitions. The MMA8450Q has user selectable full scales of ±2g/±4g/±8g. The device can be configured to generate inertial wake-up interrupt signals from any combination of the configurable embedded functions allowing the MMA8450Q to monitor events and remain in a low power mode during periods of inactivity. The MMA8450Q is available in a 3 x 3 x 1 mm QFN package.

Top View



Pin Connections

Features

- 1.71 V to 1.89 V supply voltage
- ±2g/±4g/±8g dynamically selectable full-scale
- Output Data Rate (ODR) from 400 Hz to 1.563 Hz
- 375 μg/√Hz noise at normal mode ODR = 400 Hz
- 12-bit digital output
- I^{2}C digital output interface (operates up to 400 kHz Fast Mode)
- Programmable 2 interrupt pins for 8 interrupt sources
- Embedded 4 channels of motion detection
  - Freefall or motion detection: 2 channels
  - Pulse Detection: 1 channel
  - Transient (Jolt) Detection: 1 channel
- Orientation (Portrait/Landscape) detection with hysteresis compensation
- Automatic ODR change for auto-wake and return-to-sleep
- 32 sample FIFO
- Self-Test
- 10,000g high shock survivability
- RoHS compliant

Typical Applications

- Static orientation detection (portrait/landscape, up/down, left/right, back/front position identification)
- Real-time orientation detection (virtual reality and gaming 3D user position feedback)
- Real-time activity analysis (pedometer step counting, freefall drop detection for HDD, dead-reckoning GPS backup)
- Motion detection for portable product power saving (auto-sleep and auto-wake for cell phone, PDA, GPS, gaming)
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)
- User interface (menu scrolling by orientation change, tap detection for button replacement

ORDERING INFORMATION

Part Number	Temperature Range	Package Drawing	Package
MMA8450QT	-40°C to +85°C	QFN-16	Tray
MMA8450QR1	-40°C to +85°C	QFN-16	Tape and Reel

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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Contents

Application Notes for Reference

The following is a list of Freescale Application Notes written for the MMA8450Q:

- **AN3915**, *Embedded Orientation Detection Using the MMA8450Q*
- **AN3916**, *Offset Calibration of the MMA8450Q*
- **AN3917**, *Motion and Freefall Detection Using the MMA8450Q*
- **AN3918**, *High Pass Filtered Data and Transient Detection Using the MMA8450Q*
- **AN3919**, *MMA8450Q Single/Double and Directional Tap Detection*
- **AN3920**, *Using the 32 Sample First In First Out (FIFO) in the MMA8450Q*
- **AN3921**, *Low Power Modes and Auto-Wake/Sleep Using the MMA8450Q*
- **AN3922**, *Data Manipulation and Basic Settings of the MMA8450Q*
- **AN3923**, *MMA8450Q Design Checklist and Board Mounting Guidelines*

1 Block Diagram and Pin Description

1.1 Block Diagram

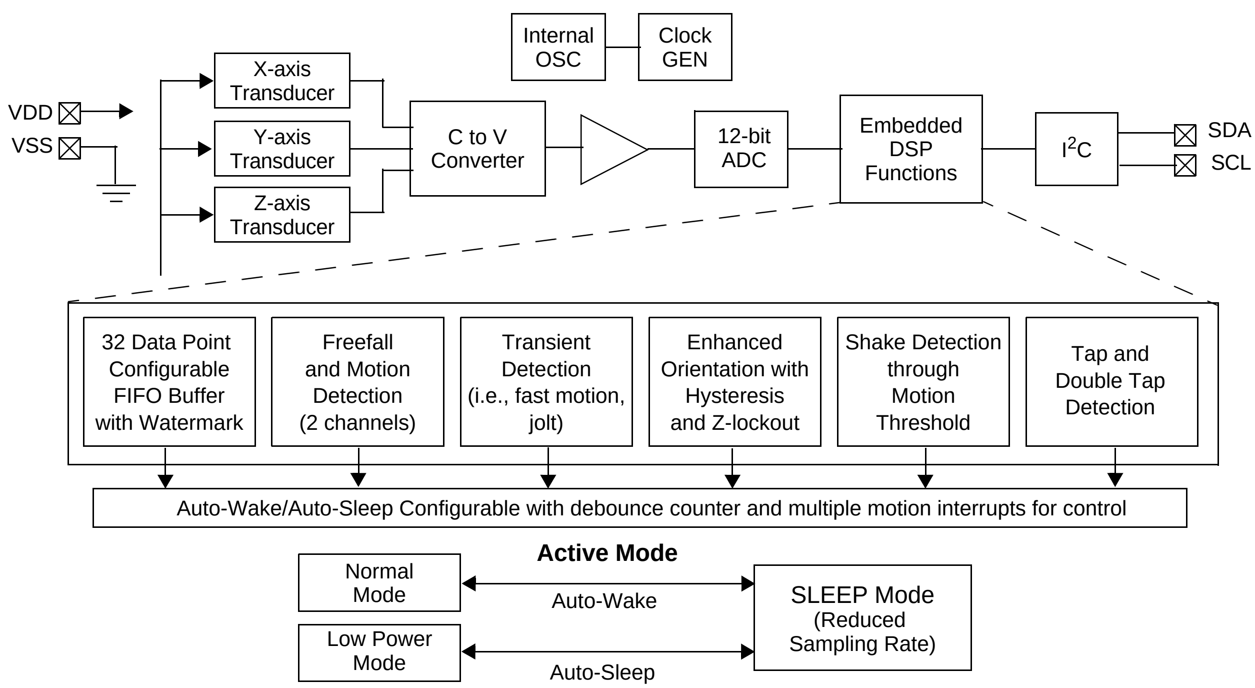


Figure 1. Block Diagram

1.2 Pin Description

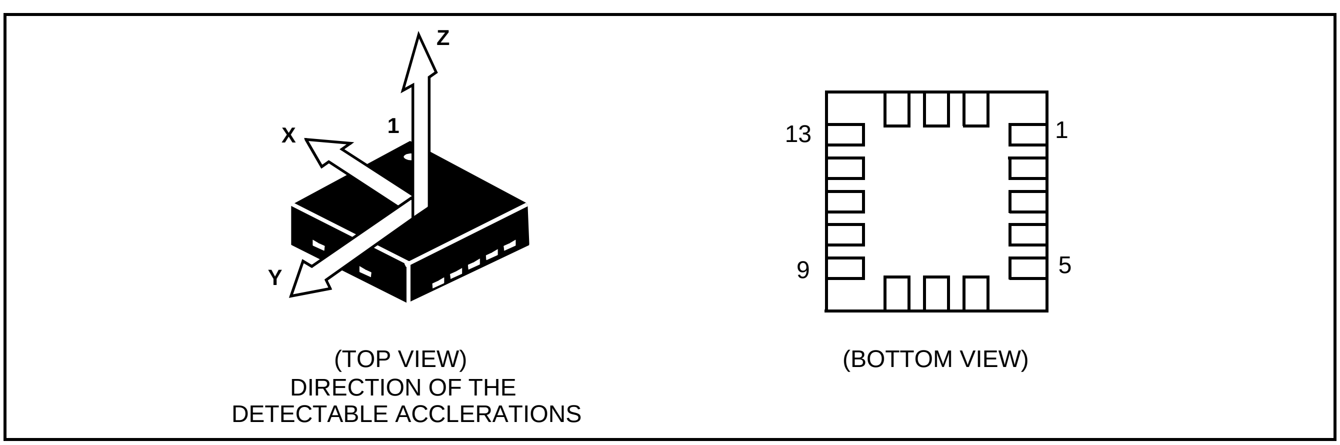


Figure 2. Direction of the Detectable Accelerations

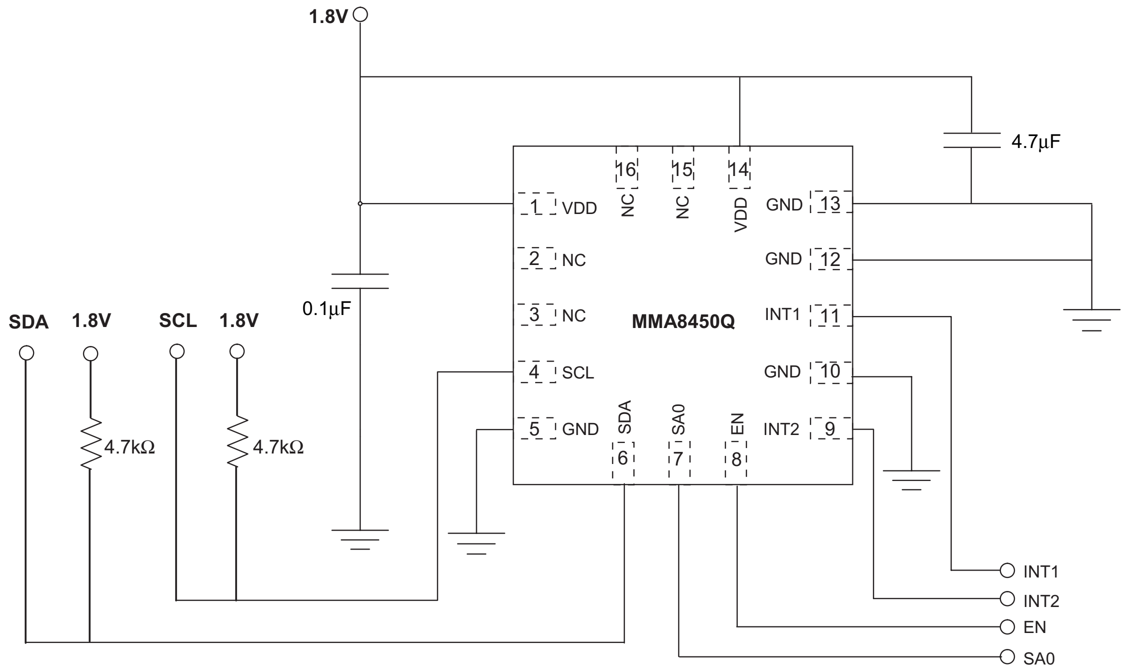


Figure 3. Application Diagram

Table 1. Pin Description

Pin #	Pin Name	Description	Pin Status
1	VDD	Power Supply (1.8V only)	Input
2	NC/GND	Connect to Ground or Non Connection	Input
3	NC/GND	Connect to Ground or Non Connection	Input
4	SCL	I^2C Serial Clock	Open Drain
5	GND	Connect to Ground	Input
6	SDA	I^2C Serial Data	Open Drain
7	SA0	I^2C Least Significant Bit of the Device Address (0: $1C 1: $1D)	Input
8	EN	Device Enable (1: I^2C Bus Enabled; 0: Shutdown Mode)	Input
9	INT2	Inertial Interrupt 2	Output
10	GND	Connect to Ground	Input
11	INT1	Inertial Interrupt 1	Output
12	GND	Connect to Ground	Input
13	GND	Connect to Ground	Input
14	VDD	Power Supply (1.8V only)	Input
15	NC	Internally not connected	Input
16	NC	Internally not connected	Input

When using MMA8450Q in applications, it is recommended that pin 1 and pin 14 (the VDD pins) be tied together. Power supply decoupling capacitors (100 nF ceramic plus 4.7 µF bulk, or a single 4.7 µF ceramic) should be placed as near as possible to the pins 1 and 5 of the device. The SDA and SCL I^2C connections are open drain and therefore require a pull-up resistor as shown in Figure 3

Note: The above application diagram presents the recommended configuration for the MMA8450Q. For information on future products of this product family please review Freescale application note, AN3923, Design Checklist and Board Mounting Guidelines of the MMA8450Q.This application note details the small modifications between the MMA8450Q and the next generation products.

1.3 Soldering Information

The QFN package is compliant with the RoHS standard. Please refer to AN3923.

2 Mechanical and Electrical Specifications

2.1 Mechanical Characteristics

Table 2. Mechanical Characteristics @ VDD = 1.8 V, T = 25°C unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Full Scale Measurement Range	FS[1:0] set to 01	FS	±1.8	±2	±2.2	g
	FS[1:0] set to 10		±3.6	±4	±4.4	
	FS[1:0] set to 11		±7.2	±8	±8.8	
Sensitivity	FS[1:0] set to 01	So	0.878	0.976	1.074	mg/digit
	FS[1:0] set to 10		1.758	1.953	2.148	
	FS[1:0] set to 11		3.515	3.906	4.296	
Sensitivity Change vs. Temperature(1)	FS[1:0] set to 01	TCSo		±0.05		%/°C
Typical Zero-g Level Offset (2)	FS[1:0] set to 01	0g-Off		±40		mg
	FS[1:0] set to 10					
	FS[1:0] set to 11					
Typical Zero-g Offset Post Board Mount (2), (3)	FS[1:0] set to 01	0g-OffBM		±50		mg
	FS[1:0] set to 10					
	FS[1:0] set to 11					
Typical Zero-g Offset Change vs. Temperature (2)		TCOff		±0.5		mg/°C
Non Linearity Best Fit Straight Line	FS[1:0] set to 01	NL		±0.25		% FS
	FS[1:0] set to 10			±0.5		
	FS[1:0] set to 11			±1		
Self-test Output Change(4)	FS[1:0] set to 01, X-axis	Vst		-195		LSB
	FS[1:0] set to 01, Y-axis			-195		
	FS[1:0] set to 01, Z-axis			+945		
Output Noise	Normal Mode ODR = 400 Hz	Noise		375		µg/√Hz
Operating Temperature Range		Top	-40		+85	°C

1. Before board mount.
2. See appendix for distribution graphs.
3. Post board mount offset specification are based on an 8 layer PCB.
4. Self-test in one direction only. These are approximate values and can change by ±100 counts.

2.2 Electrical Characteristics

Table 3. Electrical Characteristics @ VDD = 1.8 V, T = 25°C unless otherwise noted.[1]

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD	1.71	1.8	1.89	V
Low Power Mode $39 CTRL_REG2: MOD[0]=1	EN = 1, ODR = 1.563 Hz	I_{dd}LP		27		µA
	EN = 1, ODR = 12.5 Hz			27		
	EN = 1, ODR = 50 Hz			27		
	EN = 1, ODR = 100 Hz			42		
	EN = 1, ODR = 200 Hz			72		
	EN = 1, ODR = 400 Hz			120		
Normal Mode $39 CTRL_REG2: MOD[0]=0	EN = 1, ODR = 1.563 Hz	I_{dd}		42		µA
	EN = 1, ODR = 12.5 Hz			42		
	EN = 1, ODR = 50 Hz			42		
	EN = 1, ODR = 100 Hz			72		
	EN = 1, ODR = 200 Hz			132		
	EN = 1, ODR = 400 Hz			225		
Current Consumption in Shutdown Mode	EN = 0	I_{dd}Sdn		<1		µA
Supply Current Drain in Standby Mode	EN = 1 and FS[1:0] = 00	I_{dd}Stby		3		µA
Digital High Level Input Voltage SCL, SDA, SA0, EN		VIH	0.75*VDD			V
Digital Low Level Input Voltage SCL, SDA, SA0, EN		VIL			0.3*VDD	V
High Level Output Voltage INT1, INT2	I_O = 500 µA	VOH	0.9*VDD			V
Low Level Output Voltage INT1, INT2	I_O = 500 µA	VOL			0.1*VDD	V
Low Level Output Voltage SDA	I_O = 500 µA	VOLS			0.1*VDD	V
Output Data Rate		ODR	0.9*ODR	ODR	1.1*ODR	Hz
Signal Bandwidth		BW		ODR/2		Hz
Boot Time from EN = 1 to Boot Complete		BT		1.55		ms
Turn-on time[1]		Ton		3/ODR		s

1. Time to obtain valid data from Standby mode to Active mode.

2.3 I²C Interface Characteristic

Table 4. I²C Slave Timing Values[1]

Parameter	Symbol	I²C Standard Mode		I²C Fast Mode		Unit
		Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Bus Free Time between STOP and START Condition	t_{BUF}	4.7		1.3		µs
Repeated START Hold Time	$t_{HD;STA}$	4		0.6		µs
Repeated START Setup Time	$t_{SU;STA}$	4.7		0.6		µs
STOP Condition Setup Time	$t_{SU;STO}$	4		0.6		µs
SDA Data Hold Time[2]	$t_{HD;DAT}$	0[3]	[4]	0[3]	[4]	µs
SDA Valid Time [5]	$t_{VD;DAT}$		3.45[4]		0.9[4]	µs
SDA Valid Acknowledge Time [6]	$t_{VD;ACK}$		3.45[4]		0.9[4]	µs
SDA Setup Time	$t_{SU;DAT}$	250		100[7]		Ns
SCL Clock Low Time	t_{LOW}	4.7		1.3		µs
SCL Clock High Time	t_{HIGH}	4		0.6		µs
SDA and SCL Rise Time	t_r		1000	$20 + 0.1C_b$[8]	300	Ns
SDA and SCL Fall Time [3][5][8][9]	t_f		300	$20 + 0.1C_b$[8]	300	Ns
Pulse width of spikes on SDA and SCL that must be suppressed by input filter	t_{SP}		50		50	Ns

1. All values referred to VIH (min) and VIL (max) levels.
2. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
5. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
6. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
7. A Fast-mode I²C device can be used in a Standard-mode I²C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
8. C_b = total capacitance of one bus line in pF.
9. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

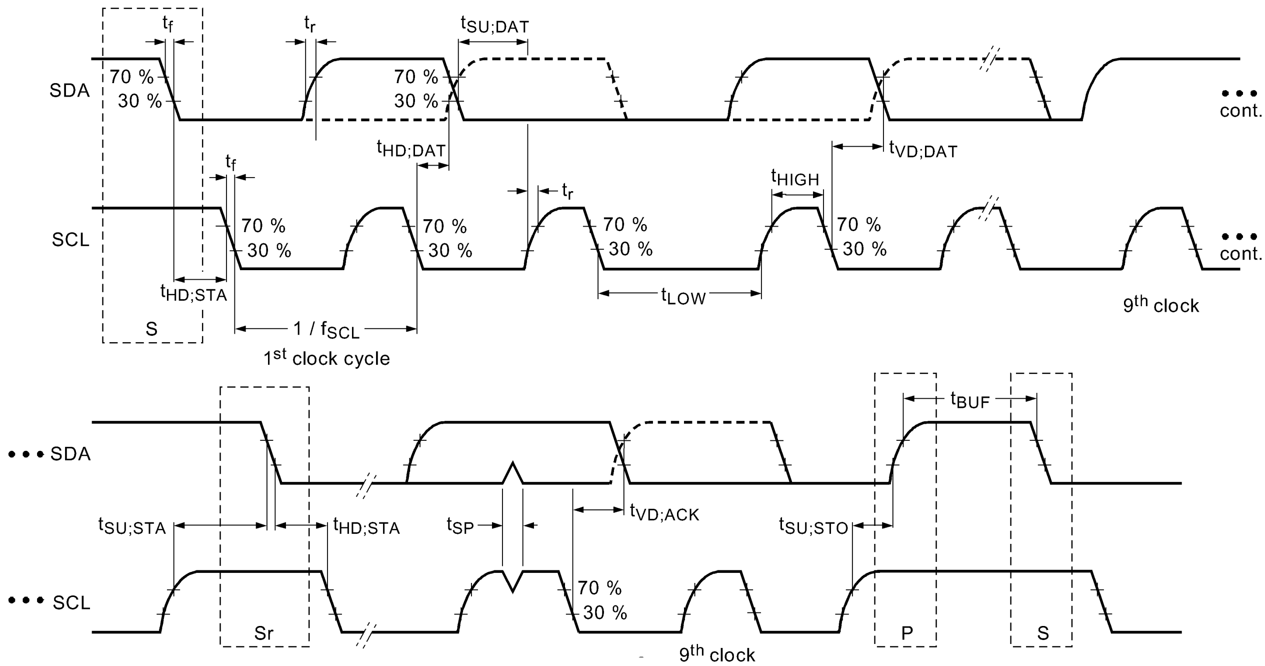


Figure 4. I²C Slave Timing Diagram

2.4 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Acceleration (all axes, 100 µs)	g_{max}	10,000	g
Supply Voltage	VDD	-0.3 to +2	V
Input voltage on any control pin (SA0, EN, SCL, SDA)	Vin	-0.3 to VDD + 0.3	V
Drop Test	D_{drop}	1.8	M
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +125	°C

Table 6. ESD and Latch-Up Protection Characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latch-up Current at T = 85°C	—	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage of the part or cause the part to otherwise fail.

This is an ESD sensitive, improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying a g acceleration to it, such as the earth's gravitational field. The sensitivity of the sensor can be determined by subtracting the -1g acceleration value from the +1g acceleration value and dividing by two.

3.2 Zero-g Offset

Zero-g Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0g in X-axis and 0g in Y-axis whereas the Z-axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 0x00, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress on the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

3.3 Self-Test

Self-Test checks the transducer functionality without external mechanical stimulus. When Self-Test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When Self-Test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

4 Modes of Operation

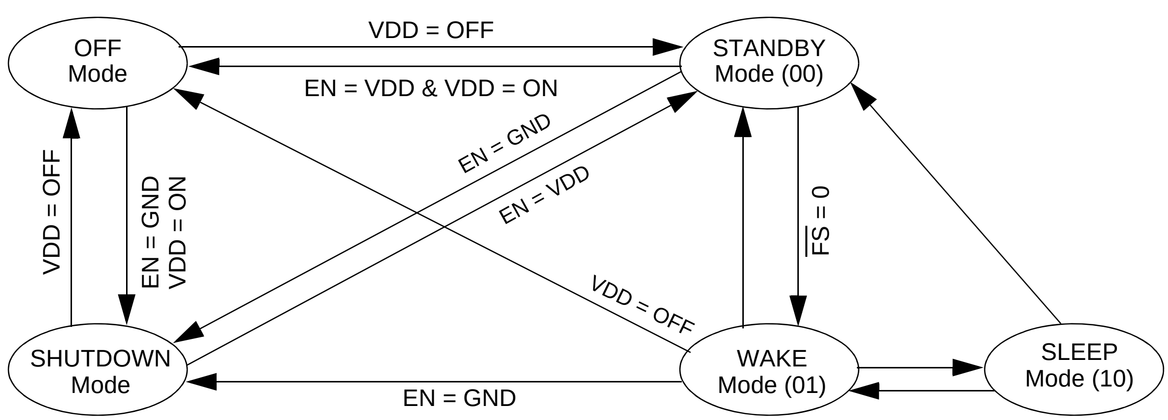


Figure 5. MMA8450Q Mode Transition Diagram

Table 7. Mode of Operation Description

Mode	I²C Bus State	VDD	EN	Function Description
OFF	Powered Down	<1.5 V	<VDD+0.3V	The device is powered off.
SHUTDOWN	I²C communication ignored	ON	EN = Low	All analog & digital blocks are shutdown.
STANDBY	I²C communication possible	ON	EN = VDD Standby register set	Only POR and digital blocks are enabled. Analog subsystem is disabled. Registers accessible for Read/Write. Device configuration done in this mode.
ACTIVE	I²C communication possible	ON	EN = VDD Standby register reset	All blocks are enabled (POR, digital, analog).

All register contents are preserved when transitioning from Active to Standby mode. Some registers are reset when transitioning from Standby to Active. These are all noted in the device memory map register table. For more detail on how to use the Sleep and Wake modes and how to transition between these modes, please refer to the functionality section of this document.

5 Functionality

The MMA8450Q is a low-power, digital output 3-axis linear accelerometer packaged in a QFN package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an I^2C serial interface. There are many embedded features in this accelerometer with a very flexible interrupt routing scheme to 2 interrupt pins including:

- 8-bit or 12-bit data, high pass filtered data, 8-bit or 12-bit configurable 32 sample FIFO
- Low power and Auto-Wake/ Sleep for conservation of current consumption
- Single and double pulse detection 1 channel
- Motion detection and Freefall 2 channels
- Transient detection based on a high pass filter and settable threshold for detecting the change in acceleration above a threshold
- Flexible user configurable portrait landscape detection algorithm addressing many use cases for screen orientation

All functionality is available in 2g, 4g or 8g dynamic ranges. There are many configuration settings for enabling all the different functions. Separate application notes have been provided to help configure the device for each embedded functionality.

5.1 Device Calibration

The IC interface is factory calibrated for sensitivity and zero-g offset for each axis. The trim values are stored in Non Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the circuitry. In normal use, further calibration in the end application is not necessary. However, the MMA8450Q allows the user to adjust the zero-g offset for each axis after power-up, changing the default offset values. The user offset adjustments are stored in 6 volatile registers. For more information on device calibration, refer to Freescale application note, AN3916*.*

5.2 8-bit or 12-bit Data

The measured acceleration data is stored in the OUTX_MSB, OUTX_LSB, OUTY_MSB, OUTY_LSB, OUTZ_MSB, and OUTZ_LSB registers as 2's complement 12-bit numbers. The most significant 8-bits of each axis are stored in OUT_X (Y, Z)_MSB, so applications needing only 8-bit results can use these 3 registers and ignore OUT_X(Y, Z)_LSB.

When the full-scale is set to 2g, the measurement range is -2g to +1.999g, and each LSB corresponds to 1g/1024 (0.98 mg) at 12-bits resolution. When the full-scale is set to 8g, the measurement range is -8g to +7.996g, and each LSB corresponds to 1g/256 (3.9 mg) at 12-bits resolution. The resolution is reduced by a factor of 16 if only the 8-bit results are used. For more information on the data manipulation between data formats and modes, refer to Freescale application note, AN3922. There is a device driver available that can be used with the Sensor Toolbox demo board (LFSTBEB8450Q) with this application note.

5.3 Internal FIFO Data Buffer

MMA8450Q contains a 32 sample internal FIFO data buffer minimizing traffic across the I2C bus. The FIFO can also provide power savings of the system by allowing the host processor/MCU to go into a sleep mode while the accelerometer independently stores the data, up to 32 samples per axis. The FIFO can run at all output data rates. There is the option of accessing the full 12-bit data for accessing only the 8-bit data. When access speed is more important than high resolution the 8-bit data flush is a better option.

The FIFO contains three modes (Fill Buffer Mode, Circular Buffer Mode, and Disabled) described in the F_SETUP Register 0x13. Fill Buffer Mode collects the first 32 samples and asserts the overflow flag when the buffer is full. It does not collect anymore data until the buffer is read. This benefits data logging applications where all samples must be collected. The Circular Buffer Mode allows the buffer to be filled and then new data replaces the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This benefits situations where the processor is waiting for an specific interrupt to signal that the data must be flushed to analyze the event.

The MMA8450Q FIFO Buffer also has a configurable watermark, allowing the processor to be interrupted after a configurable number of samples has filled in the buffer (1 to 32).

For details on the configurations for the FIFO Buffer as well as more specific examples and application benefits, refer to Freescale application note, AN3920*.*

5.4 Low Power Mode

The MMA8450Q can be set to a low power mode option to further reduce the current consumption of the device. When the Low Power Mode is enabled, the device has access to all the configurable sampling rates and features as is available in the Normal power mode. To set the device into Low Power Mode, bit 0 in the System Control Register 2 (0x39) should be set (1) (this bit is cleared (0) for Normal Power Mode). Low Power Mode reduces the current consumption by internally sleeping longer and averaging the data less. The Low Power Mode is an additional feature that is independent of the sleep feature.The sleep feature can also be used to reduce the current consumption by automatically changing to a lower sample rate when no activity is detected.

For more information on how to configure the MMA8450Q in Low Power Mode and the power consumption benefits of Low Power Mode and Auto-Wake/Sleep with specific application examples, refer to Freescale application note, AN3921.

5.5 Auto-Wake/Sleep Mode

The MMA8450Q can be configured to transition between sample rates (with their respective current consumption) based on five of the interrupt functions of the device. The advantage of using the Auto-Wake/Sleep is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the Sleep Mode (lower current) when the device does not require higher sampling rates. Auto-Wake refers to the device being triggered by one of the interrupt functions to transition to a higher sample rate. This may also interrupt the processor to transition from a sleep mode to a higher power mode.

Sleep Mode occurs after the accelerometer has not detected an interrupt for longer than the user definable time-out period. The device will transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode to save on current during this period of inactivity.

The Interrupts that can wake the device from sleep are the following: Tap Detection, Orientation Detection, Motion/Freefall1, Motion/Freefall2, and Transient Detection. The FIFO can be configured to hold the data in the buffer until it is flushed if the FIFO Gate bit is set in Register 0x3A but the FIFO cannot wake the device from sleep.

The interrupts that can keep the device from falling asleep are the same interrupts that can wake the device with the addition of the FIFO. If the FIFO interrupt is enabled and data is being accessed continually servicing the interrupt then the device will remain in the wake mode. Refer to AN3921, for more detailed information for configuring the Auto-Wake/Sleep and for application examples of the power consumption savings.

5.6 Freefall and Motion Detection

MMA8450Q has flexible interrupt architecture for detecting Freefall and Motion with the two Motion/Freefall interrupt functions available. With two configurable interrupts for Motion and Freefall, one interrupt can be configured to detect a linear freefall while the other can be configured to detect a spin motion. The combination of these two events can be routed to separate interrupts or to the same interrupt pin to detect tumble which is the combination of spin with freefall. For details on the advantages of having the two embedded functions of Freefall and Motion detection with specific application examples with recommended configuration settings, refer to Freescale application note AN3917.

5.6.1 Freefall Detection

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is **below** a user specified threshold for a user definable amount of time. Normally the usable threshold ranges are between ±0 mg and ±500 mg.

5.6.2 Motion Detection

There are two programmable functions for motion (MFF1 and MFF2). Motion is configured using the high-g mechanism. Motion is often used to simply alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event. The motion detection function can analyze static acceleration changes or faster jolts. For example, to detect that an object is spinning, all three axes would be enabled with a threshold detection of > 2g. This condition would need to occur for a minimum of 100 ms to ensure that the event wasn't just noise. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to determine whether the condition exists for configurable set of time (i.e., 100 ms or longer).

5.7 Transient Detection

The MMA8450Q has a built in high pass filter. Acceleration data goes through the high pass filter, eliminating the offset (DC) and low frequencies. The high pass filter cut-off frequency can be set by the user to four different frequencies which are dependent on the Output Data Rate (ODR). A higher cut-off frequency ensures the DC data or slower moving data will be filtered out, allowing only the higher frequencies to pass. The embedded Transient Detection function uses the high pass filtered data allowing the user to set the threshold and debounce counter.

Many applications use the accelerometer’s static acceleration readings (i.e., tilt) which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered from a low pass filter where high frequency data is considered noise. However, there are many functions where the accelerometer must analyze dynamic acceleration. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the acceleration. It is simpler to interpret these functions dependent on dynamic acceleration data when the static component has been removed. The Transient Detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 Register (0x3C). Registers 0x2B – 0x2E are the dedicated Transient Detection configuration registers. For details on the benefits of the embedded Transient Detection function along with specific application examples and recommended configuration settings, please refer to Freescale application note, AN3918.

5.8 Orientation Detection

The MMA8450Q incorporates an advanced algorithm for orientation detection (ability to detect all 6 orientations including portrait/landscape) with a large amount of configuration available to provide extreme flexibility to the system designer. The configurability also allows for the function to work differently for various modes of the end system. For example, the MMA8450Q Orientation Detection allows up to 10 selectable trip angles for Portrait-to-Landscape, up to10 selectable trip angles for the transition for Landscape-to-Portrait, and 4 selectable front/back trip angles. Typically the desired hysteresis angle is ±15° from a 45° trip reference point, resulting in |30°| and |60°| trip points. The algorithm is robust enough to handle typical process variation and uncompensated board mount offset, however, it may result in slight angle variations.

The MMA8450Q Orientation Detection algorithm confirms the reliability of the function with a configurable Z-lock out angle. Based on known functionality of linear accelerometers, it is not possible to rotate the device about the Z-axis to detect change in acceleration at slow angular speeds. The angle at which the image no longer detects the orientation change is referred to as the “Z-Lock- out angle”. The MMA8450Q Orientation Detection function has eight selectable1g-lockout thresholds; and there are 8 different settings for the Z-Angle lockout.

The Orientation Detection function also considers when a device is experiencing acceleration above a set threshold not typical of orientation changes (i.e., When a person is jogging or due to acceleration changes from being on a bus or in a car). The screen orientation should not interpret this as a change and the screen should lock in the last known valid position. This added feature, called the 1g Lockout Threshold, enhances the Orientation Detection function and confirms the reliability of the algorithm for the system. The MMA8450Q allows for configuring the 1g Lockout Threshold from 1g up to 1.35g (in increments of 0.05g).

For further information on the highly configurable embedded Orientation Detection Function, including recommendations for configuring the device to support various application use cases, refer to Freescale application note, AN3915.

Figure 6 and Figure 7 show the definitions of the trip angles going from Landscape-to-Portrait and then also from Portrait-to-Landscape.

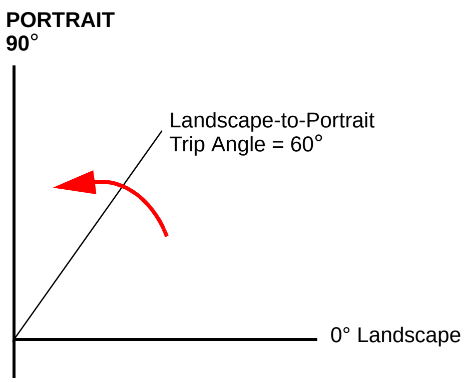


Figure 6. Illustration of Landscape-to-Portrait Transition

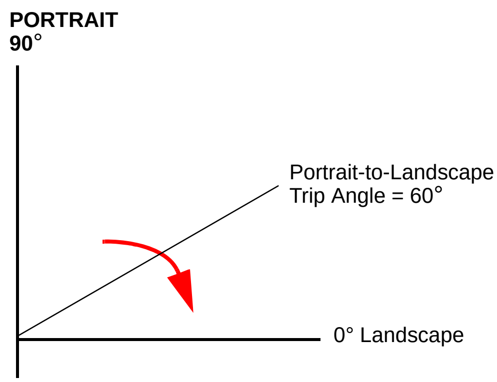


Figure 7. Illustration of Portrait-to-Landscape Transition

Figure 8 illustrates the Z-angle lockout region. When lifting the device up from the flat position it will be active for orientation detection as low as 25° from flat. This is user configurable. The default angle is 32° but it can be set as low as 25°.

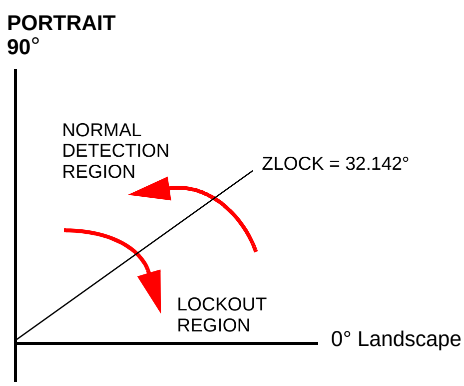


Figure 8. Illustration of Z-Tilt Angle Lockout Transition

Figure 9 shows the device configuration in the 6 different orientation modes. These orientations are defined as the following: PU = Portrait UP, LR = Landscape Right, PD = Portrait Down, LL = Landscape Left, Back and Front.

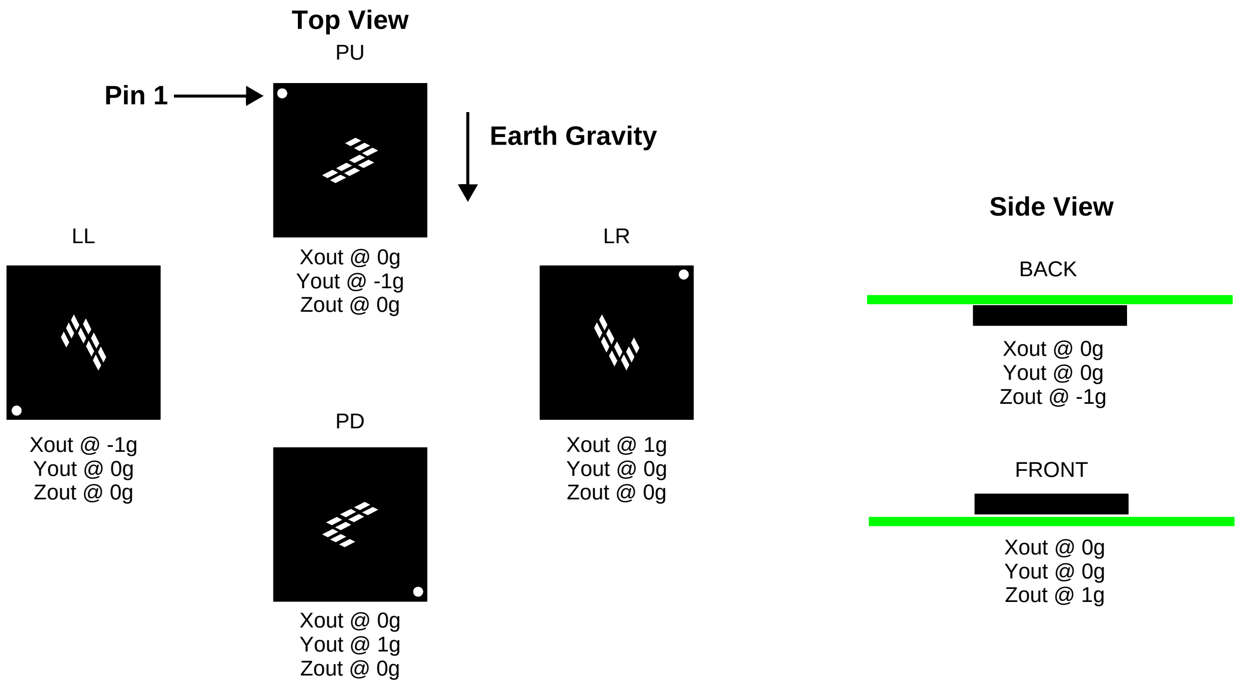


Figure 9. Landscape/Portrait Orientation

There are several registers to configure the orientation detection and are described in detail in the register setting section.

5.9 Interrupt Register Configurations

There are eight configurable interrupts in the MMA8450Q. These are Auto-Sleep, Data Ready, Motion/Freefall 1, Motion/ Freefall 2, Transient, Orientation Detection, Tap Detection and the FIFO events. These eight interrupt sources can be routed to one of two interrupt pins. The interrupt source must be enabled and configured. If the event flag is asserted because the event condition is detected, the corresponding interrupt pin, INT1 or INT2, will assert.

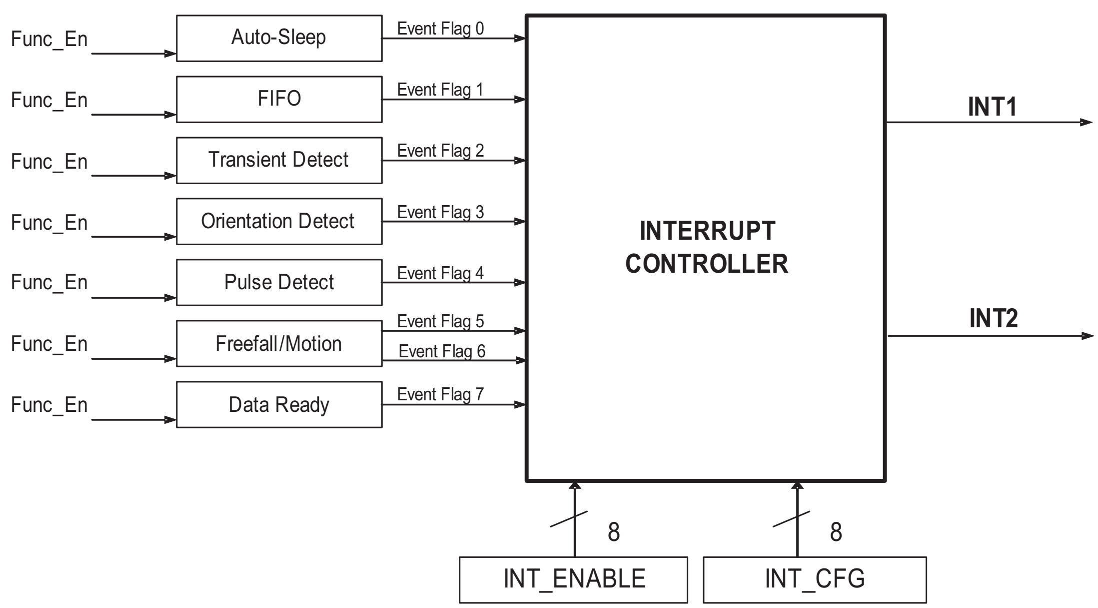


Figure 10. System Interrupt Generation Block Diagram

5.10 Serial I^{2}C Interface

Acceleration data may be accessed through an I^{2}C interface thus making the device particularly suitable for direct interfacing with a microcontroller. The MMA8450Q features an interrupt signal which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device. The MMA8450Q may also be configured to generate other interrupt signals accordingly to the programmable embedded functions of the device for Motion, Freefall, Transient, Orientation, and Tap.

The registers embedded inside MMA8450Q are accessed through an I^{2}C serial interface. To enable the I^{2}C interface, the EN pin (pin 8) must be tied high. When EN is tied low, MMA8450Q is put into low power shutdown mode and communications on the I^{2}C interface are ignored. The MMA8450Q is always in slave mode. The I^{2}C interface may be used for communications between other I^{2}C devices when EN is tied low and the MMA8450Q does not clamp the I^{2}C bus.

Table 8. Serial Interface Pin Description

Pin Name	Pin Description
EN	Device enable (1: I^{2}C mode enabled; 0: Shutdown mode)
SCL	I^{2}C Serial Clock
SDA	I^{2}C Serial Data
SA0	I^{2}C least significant bit of the device address

There are two signals associated with the I^{2}C bus; the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External 4.7 kΩ pull-up resistors connected to VDD are expected for SDA and SCL. When the bus is free both the lines are high. The I^{2}C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I^{2}C standards (Table 4).

5.10.1 I^{2}C Operation

The transaction on the bus is started through a start condition (START) signal. START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After START has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master. The 9th clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes transferred per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching.

A LOW to HIGH transition on the SDA line while the SCL line is high is defined as a stop condition (STOP). A data transfer is always terminated by a STOP. A Master may also issue a repeated START during a data transfer. The MMA8450Q expects repeated STARTs to be used to randomly read from specific registers.

The MMA8450Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request. The format is shown in Table 9.

Table 9. I^{2}C Address Selection Table

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0011100	0011101	Factory Default

Single Byte Read

The MMA8450Q has an internal ADC that can sample, convert and return sensor data on request. The transmission of an 8-bit command begins on the falling edge of SCL. After the eight clock cycles are used to send the command, note that the data returned is sent with the MSB first once the data is received. Figure 11 shows the timing diagram for the accelerometer 8-bit I^{2}C read operation. The Master (or MCU) transmits a start condition (ST) to the MMA8450Q, slave address ($1D), with the R/W bit set to “0” for a write, and the MMA8450Q sends an acknowledgement. Then the Master (or MCU) transmits the address of the register to read and the MMA8450Q sends an acknowledgement. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8450Q ($1D) with the R/W bit set to “1” for a read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NAK) it received the transmitted data, but transmits a stop condition to end the data transfer.

Multiple Byte Read

When performing a multi-byte read or "burst read", the MMA8450Q automatically increments the received register address commands after a read command is received. Therefore, after following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8450Q acknowledgment (AK) is received until a NACK is received from the Master followed by a stop condition (SP) signaling an end of transmission.

Single Byte Write

To start a write command, the Master transmits a start condition (ST) to the MMA8450Q, slave address ($1D) with the R/W bit set to "0" for a write, the MMA8450Q sends an acknowledgement. Then the Master (MCU) transmits the address of the register to write to, and the MMA8450Q sends an acknowledgement. Then the Master (or MCU) transmits the 8-bit data to write to the designated register and the MMA8450Q sends an acknowledgement that it has received the data. Since this transmission is complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA8450Q is now stored in the appropriate register.

Multiple Byte Write

The MMA8450Q automatically increments the received register address commands after a write command is received. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA8450Q acknowledgment (ACK) is received.

Table 10. I²C device Address Sequence

Command	[6:1] Device Address	[0] SA0	[6:0] Device Address	R/W	8-bit Final Value
Read	001110	0	0x1C	1	0x39
Write	001110	0	0x1C	0	0x38
Read	001110	1	0x1D	1	0x3B
Write	001110	1	0x1D	0	0x3A

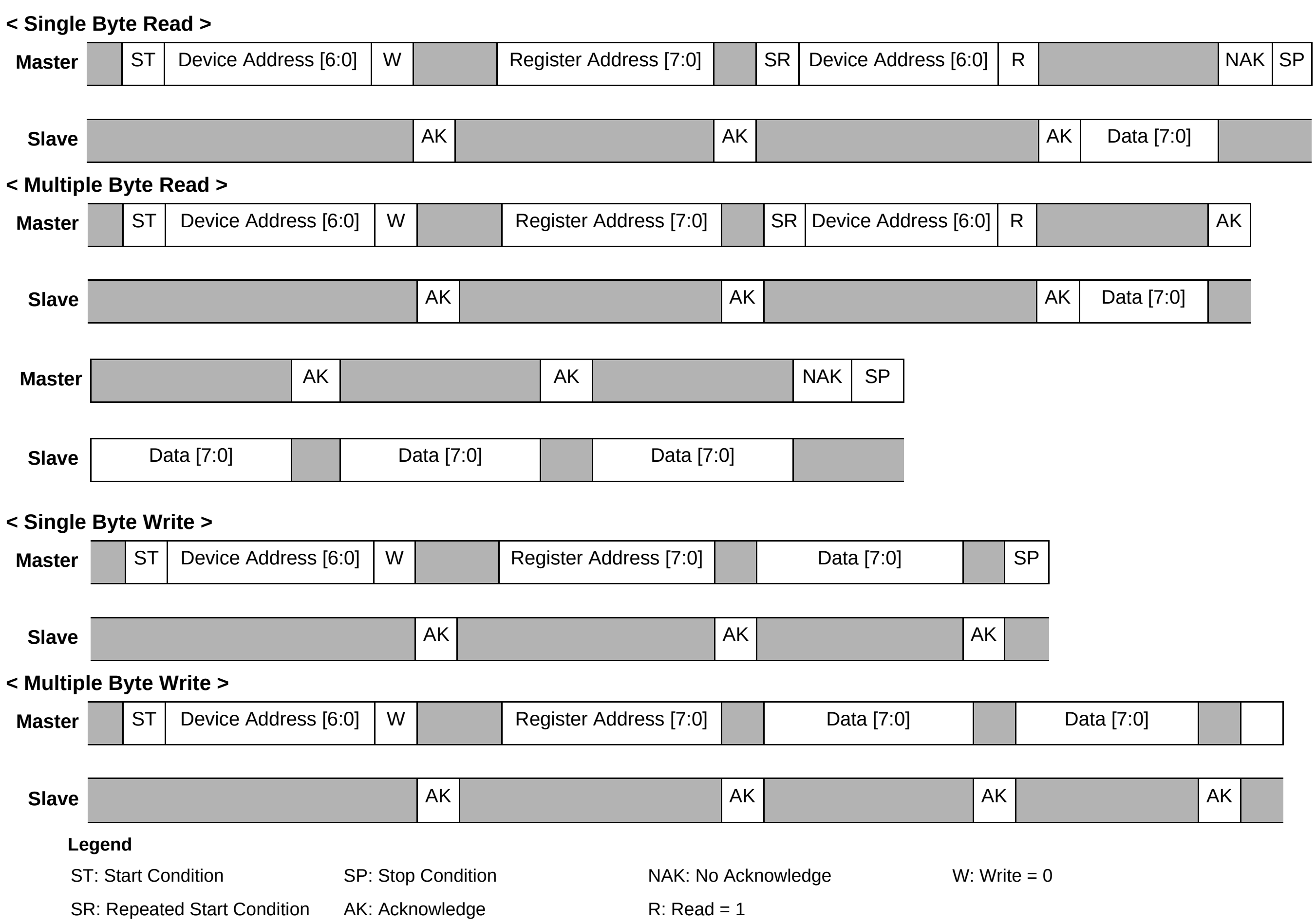


Figure 11. I²C Timing Diagram

6 Register Descriptions

Table 11 is the memory map of the MMA8450Q.The user has access to all addresses from 0x00 to 0x3F.

Table 11. Register Address Map

Name	Type	Register Address	Auto-Increment Address		Default	Comment	
STATUS[1][2]	R	0x00	0x01		00000000	Addresses 0x00, 0x04, 0x0B are aliases to the same register. Data Ready status information or FIFO status information.	
OUT_X_MSB[1][2]	R	0x01	0x02	0x01	output	[7:0] are 8 MSBs of 12-bit real-time sample.	Root pointer to XYZ FIFO 8-bit data.
OUT_Y_MSB[1][2]	R	0x02	0x03		output	[7:0] are 8 MSBs of 12-bit real-time sample	
OUT_Z_MSB[1][2]	R	0x03	**0x00**		output	[7:0] are 8 MSBs of 12-bit real-time sample	
STATUS[1][2]	R	0x04	0x05		00000000	Addresses 0x00, 0x04, 0x0B are aliases to the same register. Data Ready status information or FIFO status information.	
OUT_X_LSB[1][2]	R	0x05	0x06	0x05	output	[3:0] are 4 LSBs of 12-bit sample.	Root pointer to XYZ FIFO 12-bit data.
OUT_X_MSB[1][2]	R	0x06	0x07		output	[7:0] are 8 MSBs of 12-bit real-time sample	
OUT_Y_LSB[1][2]	R	0x07	0x08		output	[3:0] are 4 LSBs of 12-bit real-time sample	
OUT_Y_MSB[1][2]	R	0x08	0x09		output	[7:0] are 8 MSBs of 12-bit real-time sample	
OUT_Z_LSB[1][2]	R	0x09	0x0A		output	[3:0] are 4 LSBs of 12-bit real-time sample	
OUT_Z_MSB[1][2]	R	0x0A	**0x04**		output	[7:0] are 8 MSBs of 12-bit real-time sample	
STATUS[1][2]	R	0x0B	0x0C		00000000	Addresses 0x00, 0x04, 0x0B are aliases to the same register. Data Ready status information or FIFO status information.	
OUT_X_DELTA[1][2]	R	0x0C	0x0D		output	8-bit AC X-axis data	
OUT_Y_DELTA[1][2]	R	0x0D	0x0E		output	8-bit AC Y-axis data	
OUT_Z_DELTA[1][2]	R	0x0E	**0x0B**		output	8-bit AC Z-axis data	
WHO_AM_I[1]	R	0x0F	0xC6		11000110	NWM Programmable Fixed Device ID No.	
F_STATUS[1][2]	R	0x10	0x11		00000000	FIFO Status: No FIFO event Detected	
F_8DATA[1][2]	R	0x11	**0x11**		Output	FIFO status and 8-bit samples	
F_12DATA[1][2]	R	0x12	**0x12**		Output	FIFO status and 12-bit samples	
F_SETUP[1][3]	R/W	0x13	0x14		00000000	FIFO setup	
SYSMOD[1][2]	R	0x14	0x15		Output	Current System Mode	
INT_SOURCE[1][2]	R	0x15	0x16		Output	Interrupt status	
XYZ_DATA_CFG[1][4]	R/W	0x16	0x17		00000000	Acceleration data event flag configuration	
HP_FILTER_CUTOFF[1,3]	R/W	0x17	0x18		00000000	Cutoff frequency is set to 4Hz @ 400Hz	
PL_STATUS[1][2]	R	0x18	0x19		00000000	Landscape/Portrait orientation status	
PL_PRE_STATUS[1][2]	R	0x19	0x1A		00000000	Landscape/Portrait previous orientation	
PL_CFG[1][4]	R/W	0x1A	0x1B		10000011	Landscape/Portrait configuration. 1g Lockout offset is set to default value of 1.15g. Debounce counters are clear during invalid sequence condition.	
PL_COUNT[1][3]	R/W	0x1B	0x1C		00000000	Landscape/Portrait debounce counter	
PL_BF_ZCOMP[1][4]	R/W	0x1C	0x1D		00000010	Back-Front Trip threshold is ±75°. Z-Lockout angle is 32.14°	
PL_P_L_THS_REG1[1][4]	R/W	0x1D	0x1E		00011010	Portrait-to-Landscape Trip Angle is 30°	

Table 11. Register Address Map

PL_P_L_THS_REG2(1)(4)	R/W	0x1E	0x1F	00100010	Portrait-to-Landscape Trip Angle is 30°
PL_P_L_THS_REG3(1)(4)	R/W	0x1F	0x20	11010100	Portrait-to-Landscape Trip Angle is 30°
PL_L_P_THS_REG1(1)(4)	R/W	0x20	0x21	00101101	Landscape-to-Portrait Trip Angle is 60°
PL_L_P_THS_REG2(1)(4)	R/W	0x21	0x22	01000001	Landscape-to-Portrait Trip Angle is 60°
PL_L_P_THS_REG3(1)(4)	R/W	0x22	0x23	10100010	Landscape-to-Portrait Trip Angle is 60°
FF_MT_CFG_1(1)(4)	R/W	0x23	0x24	00000000	Freefall/Motion1 configuration
FF_MT_SRC_1(1)(2)	R	0x24	0x25	00000000	Freefall/Motion1 event source register
FF_MT_THS_1(1)(3)	R/W	0x25	0x26	00000000	Freefall/Motion1 threshold register
FF_MT_COUNT_1(1)(3)	R/W	0x26	0x27	00000000	Freefall/Motion1 debounce counter
FF_MT_CFG_2(1)(4)	R/W	0x27	0x28	00000000	Freefall/Motion2 configuration
FF_MT_SRC_2(1)(2)	R	0x28	0x29	00000000	Freefall/Motion2 event source register
FF_MT_THS_2(1)(3)	R/W	0x29	0x2A	00000000	Freefall/Motion2 threshold register
FF_MT_COUNT_2(1)(3)	R/W	0x2A	0x2B	00000000	Freefall/Motion2 debounce counter
TRANSIENT_CFG(1)(4)	R/W	0x2B	0x2C	00000000	Transient configuration
TRANSIENT_SRC(1)(2)	R	0x2C	0x2D	00000000	Transient event status register
TRANSIENT_THS(1)(3)	R/W	0x2D	0x2E	00000000	Transient event threshold
TRANSIENT_COUNT(1)(3)	R/W	0x2E	0x2F	00000000	Transient debounce counter
PULSE_CFG(1)(4)	R/W	0x2F	0x30	00000000	ELE, Double_XYZ or Single_XYZ
PULSE_SRC(1)(2)	R	0x30	0x31	00000000	EA, Double_XYZ or Single_XYZ
PULSE_THSX(1)(3)	R/W	0x31	0x32	00000000	X and Y pulse threshold
PULSE_THSY(1)(3)	R/W	0x32	0x33	00000000	Z pulse threshold
PULSE_THSZ(1)(3)	R/W	0x33	0x34	00000000	Z pulse threshold
PULSE_TMLT(1)(4)	R/W	0x34	0x35	00000000	Time limit for pulse
PULSE_LTCY(1)(4)	R/W	0x35	0x36	00000000	Latency time for 2nd pulse
PULSE_WIND(1)(4)	R/W	0x36	0x37	00000000	Window time for 2nd pulse
ASLP_COUNT(1)(4)	R/W	0x37	0x38	00000000	Counter setting for auto-sleep
CTRL_REG1(1)(4)	R/W	0x38	0x39	00000000	ODR = 400Hz, Standby Mode.
CTRL_REG2(1)(4)	R/W	0x39	0x3A	00000000	ST = Disabled, SLPE = Disabled, MODS = normal mode.
CTRL_REG3(1)(4)	R/W	0x3A	0x3B	00000000	IPOL, PP_OD
CTRL_REG4(1)(4)	R/W	0x3B	0x3C	00000000	Interrupt enable register
CTRL_REG5(1)(4)	R/W	0x3C	0x3D	00000000	Interrupt pin (INT1/INT2) map configuration
OFF_X(1)(4)	R/W	0x3D	0x3E	00000000	X-axis offset adjust
OFF_Y(1)(4)	R/W	0x3E	0x3F	00000000	Y-axis offset adjust
OFF_Z(1)(4)	R/W	0x3F	**0x0F**	00000000	Z-axis offset adjust

1. Register contents are preserved when transition from “ACTIVE” to “STANDBY” mode occurs.
2. Register contents are reset when transition from “STANDBY” to “ACTIVE” mode occurs.
3. Modification of this register’s contents can only occur when device is “STANDBY” mode
4. Register contents can be modified anytime in “STANDBY” or “ACTIVE” mode. A write to this register will cause a reset of the corresponding internal system debounce counter.

Note: Auto-increment addresses which are not a simple increment are highlighted in **bold**. The auto-increment addressing is only enabled when device registers are read using I^2C burst read mode. Therefore the internal storage of the auto-increment address is clear whenever a stop-bit is detected.

6.1 Data Registers

The following are the data registers for the MMA8450Q. For more information on data manipulation of the MMA8450Q, refer to application note, AN3922.

0x00, 0x04, 0x0B: STATUS Registers

Alias for DR_Status (0x0B) or F_Status (0x10) (Read Only)

FDE (FIFO Data Enable Bit 7, Reg 0x16) Setting	Alias Status
FDE = 0	0x00 = 0x04 = DR_STATUS (0x0B)
FDE = 1	0x00 = 0x04 = F_STATUS (0x10)

When FDE bit found in register 0x16 (XYZ_DATA_CFG), bit 7 is cleared (the FIFO is not on) register 0x00, 0x04 and 0x0B should all be the same value and reflect the real-time status information of the X, Y and Z sample data. When FDE is set (the FIFO is on) Register 0x00, 0x04 and 0x10 will have the same value and 0x0B will reflect the status of the transient data. The aliases allow the STATUS register to be read easily before reading the current 8-bit, 12-bit, or FIFO sample data using the register address auto-incrementing mechanism.

0X00, 0X04, 0X0B STATUS: Data Status Registers (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Table 12. STATUS Description

ZYXOW	X, Y, Z-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous X, Y, or Z data was overwritten by new X, Y, or Z data before it was read
ZOW	Z-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous Z-axis data was overwritten by new Z-axis data before it was read
YOW	Y-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous Y-axis data was overwritten by new Y-axis data before it was read
XOW	X-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous X-axis data was overwritten by new X-axis data before it was read
ZYXDR	X, Y, Z-axis new Data Ready. Default value: 0 0: No new set of data ready 1: A new set of data is ready
ZDR	Z-axis new Data Available. Default value: 0 0: No new Z-axis data is ready 1: A new Z-axis data is ready
YDR	Z-axis new Data Available. Default value: 0 0: No new Y-axis data ready 1: A new Y-axis data is ready
XDR	Z-axis new Data Available. Default value: 0 0: No new X-axis data ready 1: A new X-axis data is ready

ZYXOW is set whenever a new acceleration data is produced before completing the retrieval of the previous set. This event occurs when the content of at least one acceleration data register (i.e., OUTX, OUTY, OUTZ) has been overwritten. ZYXOW is cleared when the high-bytes of the acceleration data (OUTX_MSB, OUTY_MSB, OUTZ_MSB) of all the active channels are read.

ZOW is set whenever a new acceleration sample related to the Z-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. ZOW is cleared anytime OUTZ_MSB register is read.

YOW is set whenever a new acceleration sample related to the Y-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. YOW is cleared anytime OUTY_MSB register is read.

XOW is set whenever a new acceleration sample related to the X-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. XOW is cleared anytime OUTX_MSB register is read.

ZYXDR signals that a new sample for any of the enabled channels is available. ZYXDR is cleared when the high-bytes of the acceleration data (OUTX_MSB, OUTY_MSB, OUTZ_MSB) of all the enabled channels are read.

ZDR is set whenever a new acceleration sample related to the Z-axis is generated. ZDR is cleared anytime OUTZ_MSB register is read. In order to enable the monitoring and assertion of this bit, the ZDR bit requires the Z-axis event detection flag to be enabled (bit ZDEFE = 1 inside XYZ_DATA_CFG register).

YDR is set whenever a new acceleration sample related to the Y-axis is available. YDR is cleared anytime OUTY_MSB register is read. In order to enable the monitoring and assertion of this bit, the YDR bit requires the Y-axis event detection flag to be enabled (bit YDEFE = 1 inside XYZ_DATA_CFG register).

XDR is set to 1 whenever a new acceleration sample related to the X-axis is available. XDR is cleared anytime OUTX_MSB register is read. In order to enable the monitoring and assertion of this bit, the XDR bit requires the X-axis to event detection flag to be enabled (bit XDEFE = 1 inside XYZ_DATA_CFG register).

The **ZDR** and **ZOW** flag generation requires the Z-axis event flag generator to be enabled (ZDEFE = 1) in the XYZ_DATA_CFG register.

The **YDR** and **YOW** flag generation requires the Y-axis event flag generator to be enabled (YDEFE = 1) in the XYZ_DATA_CFG register.

The **XDR** and **XOW** flag generation requires the X-axis event flag generator to be enabled (XDEFE = 1) in the XYZ_DATA_CFG register.

The **ZYXDR** and **ZYXOW** flag generation is requires the Z-axis, Y-axis, X-axis event flag generator to be enabled (ZDEFE = 1, YDEFE = 1, XDEFE = 1) in the XYZ_DATA_CFG register.

0x01, 0x02, 0x03: OUT_MSB 8-Bit XYZ Data Registers

X, Y and Z-axis data is expressed as 2's complement numbers. The most significant 8-bits are stored together in OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB so applications needing only 8-bit results can use these registers and can ignore the OUT_X_LSB, OUT_Y_LSB, OUT_Z_LSB. The status Register 0x00, OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB are duplicated in the auto-incrementing address range of 0x00 to 0x03 to reduce reading the status followed by 8-bit axis data to a 4 byte sequence.

0x01 OUT_X_MSB: X_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4

0x02 OUT_Y_MSB: Y_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4

0x03 OUT_Z_MSB: Z_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4

0x05 - 0x0A: OUT_MSB and OUT_LSB 12-Bit XYZ Data Registers

X, Y and Z-axis data is expressed as 2's complement numbers. The STATUS (0x04), OUT_X_LSB (0x05), OUT_X_MSB (0x06), OUT_Y_LSB (0x07), OUT_Y_MSB (0x08), OUT_Z_LSB(0x09), OUT_Z_MSB (0x0A) are stored in auto-incrementing address range of 0x04 to 0x0A to reduce reading the status followed by 12-bit axis data to 7 bytes.

0x05 OUT_X_LSB: X_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	XD3	XD2	XD1	XD0

0x06 OUT_X_MSB: X_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4

0x07 OUT_Y_LSB: Y_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	YD3	YD2	YD1	YD0

0x08 OUT_Y_MSB: Y_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4

0x09 OUT_Z_LSB: Z_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	ZD3	ZD2	ZD1	ZD0

0x0A OUT_Z_MSB: Z_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4

The sample data output registers store the current sample data if the FIFO data output register driver is disabled, but if the FIFO data output register driver is enabled,12 the sample data output registers point to the head of the FIFO buffer which contains the previous 32 X, Y, and Z data samples. This applies for the 8-bit data and the 12-bit data.

When the FDE bit is set to logic 1, the F_8DATA (0x11) FIFO root data pointer shares the same address location as the OUT_X_MSB register (0x01); therefore all 8-bit accesses of the FIFO buffer data must use the I^2C address 0x01. The F_12DATA (0x12) FIFO root data pointer shares the same address location as the OUT_X_LSB register (0x05); therefore all 12-bit accesses of the FIFO buffer data must use the I^2C address 0x05. All reads to register addresses 0x02, 0x03, 0x06, 0x07, 0x08, 0x09, and 0x0A returns a value of 0x00.

0x0C - 0x0E: OUT_X_DELTA, OUT_Y_DELTA, OUT_Z_DELTA AC Data Registers

X, Y, and Z-axis 8-bit high pass filtered output data is expressed as 2's complement numbers. The data is obtained from the output of the user definable high pass filter. The data cuts out the low frequency data, which is useful in that the offset data is removed. The value of the high pass filter cut off frequency is set in Register 0x17.

Note: The OUT_X_DELTA, OUT_Y_DELTA, OUT_Z_DELTA registers store the high pass filtered “delta data” information regardless of the state of the FIFO data output register driver bit. Register 0x0B always reflects the status of the delta data.

0x0C OUT_X_DELTA: AC X 8-Bit Data Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

0x0D OUT_Y_DELTA: AC Y 8-Bit Data Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

0x0E OUT_Z_DELTA: AC Z 8-Bit Data Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

0x0F: WHO_AM_I Device ID Register

This register contains the device identifier which for MMA8450Q is set to **0xC6** by default. The value is factory programmed by a byte of NVM. A custom alternate value can be set by customer request.

0x0F WHO_AM_I: Device ID Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	0	1	1	0

6.2 32 Sample FIFO

The following registers are used to configure the FIFO. The following are the FIFO registers for the MMA8450Q. For more information on the FIFO please refer to AN3920.

0x10: F_STATUS FIFO Status Register

The FIFO Status Register is used to retrieve information about the FIFO. This register has a flag for the overflow and watermark. It also has a counter that can be read to obtain the number of samples stored in the buffer.

0x10 F_STATUS: FIFO STATUS Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_OVF	F_WMRK_FLAG	F_CNT5	F_CNT4	F_CNT3	F_CNT2	F_CNT1	F_CNT0

Table 13. FIFO Flag Event Description

F_OVF	F_WMRK_FLAG	Event Description
0	—	No FIFO overflow events detected.
1	—	FIFO event detected; FIFO has overflowed.
—	0	No FIFO watermark events detected.
—	1	FIFO event detected; FIFO sample count is greater than watermark value.

The F_OVF and F_WMRK_FLAG flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit flag in the interrupt source register (INT_SOURCE) by reading the F_STATUS register.

Therefore the F_OVF bit flag will remain asserted while the FIFO has overflowed and the F_WMRK_FLAG bit flag will remain asserted while the F_CNT value is greater than the F_WMRK value.

Table 14. FIFO Sample Count Description

F_CNT[5:0]	FIFO sample counter. Default value 00_0000. (00_0001 to 10_0000 indicates 1 to 32 samples stored in FIFO

F_CNT[5:0] bits indicate the number of acceleration samples currently stored in the FIFO buffer. Count 000000 indicates that the FIFO is empty.

0x11: F_8DATA 8-Bit FIFO Data

F_8DATA provides access to the previous (up to) 32 samples of X, Y, and Z-axis acceleration data at 8-bit resolution. Use F_12DATA to access the same FIFO data at 12-bit resolution. The advantage of F_8DATA access is much faster download of the sample data, since it is represented by only 3 bytes per sample (OUT_X_MSB, OUT_Y_MSB, and OUT_Z_MSB).

All reads to address 0x01 returns the sensor sampled data in the FIFO buffer, 3 bytes per sample (one byte per axis), with the oldest samples first, in order OUT_X_MSB, OUT_Y_MSB, and OUT_Z_MSB. When all samples indicated by the FIFO_Status register have been read from the FIFO, subsequent reads will return 0x00. Since the FIFO holds a maximum of 32 samples, a maximum of 3 x 32 = 96 data bytes of samples can be read.

The FIFO will not accumulate more sample data during an access to F_8DATA until a STOP or repeated START occurs.

0x11 F_8DATA: 8-Bit FIFO Data Register Points to Register 0x01 (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4

The host application should initially perform a single byte read of the FIFO status byte (address 0x10) to determine the status of the FIFO and if it is determined that the FIFO contains data sample(s), the FIFO contents can also be read from register address location 0x01 or 0x05.

0x12: F_12DATA 12-Bit FIFO Data

F_12DATA provides access to the previous (up to) 32 samples of X, Y, and Z-axis acceleration data, at 12-bit resolution. Use F_8DATA to access the same FIFO data at 8-bit resolution. The advantage of F_8DATA access is much faster download of the sample data, since it is represented by only 3 bytes per sample (OUT_X_MSB, OUT_Y_MSB, and OUT_Z_MSB).

When the FDE bit is set to logic 1, the F_12DATA FIFO root data pointer shares the same address location as the OUT_X_MSB register (0x05); therefore all 12-bit accesses of the FIFO buffer data must use the I^2C register address 0x05. All reads to the register address 0x02, 0x03, 0x06, 0x07, 0x08, 0x09, and 0x0A return a value of 0x00.

All reads from address (0x05) return the sample data, oldest samples first, in order OUT_X_LSB OUT_X_MSB, OUT_Y_LSB, OUT_Y_MSB, OUT_Z_LSB, and OUT_Z_MSB. When all samples indicated by the F_Status byte have been read from the FIFO, subsequent reads will return 0x00. Since the FIFO holds a maximum of 32 samples, a maximum of 6 x 32 = 192 data bytes can be read.

The FIFO will not accumulate more sample data during an access to F_12DATA until a STOP or repeated START occurs.

0x12 F_12DATA: 12-Bit FIFO Data Register Points to Register 0x05 (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	XD3	XD2	XD1	XD0

0x13: F_SETUP FIFO Setup Register

This setup register is used to configure the options for the FIFO. The FIFO can operate in 3 states which are defined in the Mode Bits. The watermark bits are configurable to set the number of samples of data to trigger the watermark event flag. The maximum number of samples is 32. For more information on the FIFO configuration refer to AN3920.

0x13 F_SETUP: FIFO Setup Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_MODE1	F_MODE0	F_WMRK5	F_WMRK4	F_WMRK3	F_WMRK2	F_WMRK1	F_WMRK0

Table 15. F_SETUP Description

BITS	Description
F_MODE[1:0](1)(2)(3)	FIFO buffer overflow mode. Default value 0. **00:** FIFO is disabled. **01:** FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample. **10:** FIFO stops accepting new samples when overflowed. **11:** Not Used. The FIFO is flushed whenever the FIFO is disabled, during an automatic ODR change (Auto-Wake/Sleep), or transitioning from “STANDBY” mode to “ACTIVE” mode. Disabling the FIFO (F_MODE = 00) resets the F_OVF, F_WMRK_FLAG, F_CNT to zero. A FIFO overflow event (i.e., F_CNT = 32) will assert the F_OVF flag and a FIFO sample count equal to the sample count watermark (i.e., F_WMRK) asserts the F_WMRK_FLAG event flag.
F_WMRK[5:0](2)	FIFO Event Sample Count Watermark. Default value 00_0000. These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag (F_WMK_FLAG) is raised when FIFO sample count F_CNT[5:0] value is equal to the F_ WMRK[5:0] watermark. Setting the F_WMRK[5:0] to 00_0000 will disable the FIFO watermark event flag generation.

1. Bit field can be written in ACTIVE mode.
2. Bit field can be written in STANDBY mode.
3. The FIFO mode (F_MODE) cannot be switched between the two operational modes (01and 10) in Active Mode.

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data. The FIFO update rate is dictated by the selected system ODR. In active mode the ODR is set by the DR register in the CTRL_REG1 register and when Auto-Sleep is active the ODR is set by the ASLP_RATE field in the CTRL_REG1 register.

When a byte is read from the FIFO buffer the oldest sample data in the FIFO buffer is returned and also deleted from the front of the FIFO buffer, while the FIFO sample count is decremented by one. It is assumed that the host application shall use the I^2C multi-read transaction to empty the FIFO.

The FIFO mode can be changed while in the active state. The mode must first be disabled F_MODE = 00 then the Mode can be changed.

0x14: SYSMOD System Mode Register

The system mode register indicates the current device operating mode. Applications using the Auto-Sleep/Auto-Wake mechanism should use this register to synchronize the application with the device operating mode transitions. The system mode register also indicates the status of the NVM parity error and FIFO gate error flags.

0x14 SYSMOD: System Mode Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PERR	FGERR	0	0	0	0	SYSMOD1	SYSMOD0

Table 16. SYSMOD Description

PERR	NVM Parity Error Flag Bit. Default Value: 0. 0: No NVM parity error was detected. 1: NVM parity error detected.
FGERR	FIFO Gate Error. Default value: 0. 0: No FIFO Gate Error detected. 1: FIFO Gate Error was detected.
SYSMOD	System Mode. Default value: 00. 00: Standby mode 01: Wake mode 10: Sleep mode

The FIFO Gate is set in Register 0x3A for the device configured for Auto-Wake/Sleep mode to allow the buffer to preserve the data without automatically flushing. If the FIFO buffer is not emptied before the arrival of the next sample, then the FGERR bit in register 0x14 is asserted. The FGERR remains asserted as long as the FIFO buffer remains un-emptied. Emptying the FIFO buffer clears the FGERR bit.

0x15: INT_SOURCE System Interrupt Status Register

In the interrupt source register the status of the various embedded features can be determined.The bits that are set (logic '1') indicate which function has asserted an interrupt and conversely the bits that are cleared (logic '0') indicate which function has not asserted or has de-asserted an interrupt. The interrupts are rising edge sensitive. The bits are set by a low to high transition and are cleared by reading the appropriate interrupt source register.

0x15 INT_SOURCE: System Interrupt Status Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT_1	SRC_FF_MT_2	SRC_DRDY

Table 17. INT_SOURCE Description

INT_SOURCE	Description
SRC_ASLP	Auto-Sleep/Wake interrupt status bit Logic '1' indicates that an interrupt event that can cause a "Wake-to-Sleep" or "Sleep-to-Wake" system mode transition has occurred. Logic '0' indicates that no "Wake-to-Sleep" or "Sleep-to-Wake" system mode transition interrupt event has occurred. **"Wake-to-Sleep"** transition occurs when no interrupt occurs for a time period that exceeds the user specified limit (ASLP_COUNT). This causes the system to transition to a user specified low ODR setting. **"Sleep-to-Wake"** transition occurs when the user specified interrupt event has woken the system; thus causing the system to transition to a user specified high ODR setting. Reading the SYSMOD register clears the SRC_ASLP bit.
SRC_FIFO	FIFO interrupt status bit Logic '1' indicates that a FIFO interrupt event such as an overflow event or watermark has occurred. Logic '0' indicates that no FIFO interrupt event has occurred. FIFO interrupt event generators: FIFO Overflow, or (Watermark: F_CNT = F_WMRK) and the interrupt has been enabled. This bit is cleared by reading the F_STATUS register.
SRC_TRANS	Transient interrupt status bit Logic '1' indicates that an acceleration transient value greater than user specified threshold has occurred. Logic '0' indicates that no transient event has occurred. This bit is asserted whenever **"**EA**"** bit in the TRANS_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the TRANS_SRC register.
SRC_LNDPRT	Landscape/Portrait Orientation interrupt status bit Logic '1' indicates that an interrupt was generated due to a change in the device orientation status. Logic '0' indicates that no change in orientation status was detected. This bit is asserted whenever **"**NEWLP**"** bit in the PL_STATUS is asserted and the interrupt has been enabled. This bit is cleared by reading the PL_STATUS register.
SRC_PULSE	Pulse interrupt status bit Logic '1' indicates that an interrupt was generated due to single and/or double pulse event. Logic '0' indicates that no pulse event was detected. This bit is asserted whenever "EA" bit in the PULSE_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the PULSE_SRC register.
SRC_FF_MT_1	Freefall/Motion1 interrupt status bit Logic '1' indicates that the Freefall/Motion1 function interrupt is active. Logic '0' indicates that no Freefall or Motion event was detected. This bit is asserted whenever "EA" bit in the FF_MT_SRC_1 register is asserted and the FF_MT interrupt has been enabled. This bit is cleared by reading the FF_MT_SRC_1 register.
SRC_FF_MT_2	Freefall/Motion2 interrupt status bit Logic '1' indicates that the Freefall/Motion2 function interrupt is active. Logic '0' indicates that no Freefall or Motion event was detected. This bit is asserted whenever "EA" bit in the FF_MT_SRC_2 register is asserted and the FF_MT interrupt has been enabled. This bit is cleared by reading the FF_MT_SRC_2 register.

Table 17. INT_SOURCE Description

SRC_DRDY	Data Ready interrupt bit status Logic '1' indicates that the X,Y,Z data ready interrupt is active indicating the presence of new data and/or data overrun. Otherwise if it is a logic '0' the X,Y,Z interrupt is not active. This bit is asserted when the ZYXOW and/or ZYXDR is set and the interrupt has been enabled. This bit is cleared by reading the STATUS and X, Y, or Z register.

0x16: XYZ_DATA_CFG Sensor Data Configuration Register

The XYZ_DATA_CFG register configures the 3-axis acceleration data and event flag generator based on the ODR.

0x16 XYZ_DATA_CFG: Sensor Data Configuration Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDE	0	0	0	0	ZDEFE	YDEFE	XDEFE

Table 18. XYZ_DATA_CFG Description

FDE	FIFO Data Output Register Driver Enable. Default value: 0. 0: The sample data output registers store the current X, Y, & Z sample data; 1: The sample data output registers point to the previously stored X, Y, & Z samples data in the FIFO buffer.
ZDEFE	Data Event Flag Enable on new Z-axis data. Default value: 0 0: Event detection disabled; 1: Raise event flag on new Z-axis data
YDEFE	Data Event Flag Enable on new Y-axis data. Default value: 0 0: Event detection disabled; 1: Raise event flag on new Y-axis data
XDEFE	Data Event Flag Enable on new X-axis data. Default value: 0 0: Event detection disabled; 1: Raise event flag on new X-axis data

0x17: HP_FILTER_CUTOFF High Pass Filter Register

This register sets the high-pass filter cut-off frequency for the detection of instantaneous acceleration. The output of this filter is indicated by the OUT_X_DELTA, OUT_Y_DELTA, and OUT_Z_DELTA registers. The filter cut-off options change based on the data rate selected as shown in Table 19. For details of implementation on the high pass filter, refer to Freescale application note AN3918.

0x17 HP_FILTER_CUTOFF: High Pass Filter Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SEL1	SEL0

Table 19. HP_FILTER_CUTOFF Setting Options

SEL1	SEL0	Fc (Hz) @ ODR = 400 Hz	Fc (Hz) @ ODR = 200 Hz	Fc (Hz) @ ODR = 100 Hz	Fc (Hz) @ ODR = 50 Hz	Fc (Hz) @ ODR = 12.5 Hz	Fc (Hz) @ ODR = 1.563 Hz
0	0	4	2	1	0.5	0.125	0.01
0	1	2	1	0.5	0.25	0.063	0.007
1	0	1	0.5	0.25	0.125	0.031	0.004
1	1	0.5	0.25	0.125	0.062	0.016	0.002

6.3 Portrait/ Landscape Embedded Function Registers

For more details on the meaning of the different user configurable settings and for example code refer to Freescale application note AN3915.

0x18: PL_STATUS Portrait/Landscape Status Register

This status register can be read to get updated information on any change in orientation by reading Bit 7, or on the specifics of the orientation by reading Bit0 to Bit 4. The interrupt for the Portrait/landscape detection is cleared by reading the status register. For further understanding of Portrait Up, Portrait Down, Landscape Left, Landscape Right, Back and Front please refer to Figure 9

0x18 PL_STATUS Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NEWLP	LO	—	LAPO[2]	LAPO[1]	LAPO[0]	BAFRO[1]	BAFRO[0]

Table 20. PL_STATUS Register Description

NEWLP	Landscape-Portrait status change flag. Default value: 0. 0: No change, 1: BAFRO and/or LAPO and/or Z-tilt lockout value has changed
LO	Z-Tilt Angle Lockout. Default value: 0. 0: Lockout condition has not been detected. 1: Z-Tilt lockout trip angle has been exceeded. Lockout has been detected.
BAFRO[1:0]	Back or Front orientation. Default value: 00 00: Undefined. This is the default power up state. 01: Front: Device is in the front facing orientation. 10: Back: Device is in the back facing orientation.
LAPO[2:0][1]	Landscape/Portrait orientation. Default value: 000 000: Undefined. This is the default power up state. 001: Portrait Up 010: Portrait Down 011: Landscape Right 100: Landscape Left

1. The default power up state is BAFRO (Undefined), LAPO (Undefined), and no Lockout for orientation function.

NEWLP is set to 1 whenever a change in LO, BAFRO, or LAPO occurs. NEWLP bit is cleared anytime PL_STATUS register is read.

0x19: PL_PRE_STATUS Portrait/Landscape Previous Data Status Register

This register provides the previous orientation data from the previous reading. These register definitions are the same as what has been described in Register 0x18.

0x19 PL_PRE_STATUS Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	LO	-—	LAPO[2]	LAPO[1]	LAPO[0]	BAFRO[1]	BAFRO[0]

0x1A: PL_CFG Portrait/Landscape Configuration Register

This register configures the behavior of the debounce counters and also sets the Landscape/Portrait 1g lockout mechanism threshold offset.

0x1A PL_CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	PL_EN	—	—	—	GOFF[2]	GOFF[1]	GOFF[0]

Table 21. PL_CFG Register Description

DBCNTM	Debounce counter mode selection. Default value: 1 0: Decrements debounce whenever condition of interest is no longer valid. 1: Clears counter whenever condition of interest is no longer valid.
PL_EN	Portrait-Landscape Detection Enable. Default value: 0 0: Portrait-Landscape Detection is Disabled. 1: Portrait-Landscape Detection is Enabled.
GOFF	1g lockout threshold offset expressed in steps of 50mg. Default value: 011 = 1.15g. The offset specified by the GOFF is added or subtracted from 1g to achieve the optimal 1g lockout threshold. If GOFF = 011, then the resulting 1g lockout threshold is ±(1g + 150mg). 000: No offset.

0x1B: PL_COUNT Portrait Landscape Debounce Register

This register sets the debounce counter for the orientation state transition. The minimum debounce latency is determined by the data rate set by the selected system ODR and PL_COUNT registers. Any change to the ODR or device mode transitioning from ACTIVE to STANDBY or vice versa resets the internal landscape/portrait internal debounce counters.

0x1B PL_COUNT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE [2]	DBNCE [1]	DBNCE [0]

The debounce counter scales with the ODR, like many of the debounce counters in the other functional blocks. Table 22 shows the relationship between the ODR, the step per count and the duration.

Table 22. PL_COUNT Relationship with the ODR

Output Data Rate (Hz)	Step	Duration Range
400	2.5 ms	2.5 ms – 0.637s
200	5 ms	5 ms – 1.275s
100	10 ms	10 ms – 2.55s
50	20 ms	20 ms – 5.1s
12.5	80 ms	80 ms – 20.4s
1.56	640 ms	640 ms – 163s

0x1C: PL_BF_ZCOMP Back/Front and Z Compensation Register

The Z-Tilt angle compensation bits allow the user to adjust the Z-lockout region from 25° up to 50°. The default Z-lockout angle is set to the default value of 32° upon power up. The Back to Front trip angle is set by default to ±75° but this angle also can be adjusted from a range of 65° to 80° with 5° step increments.

0x1C: PL_BF_ZCOMP Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BKFR[1]	BKFR[0]	—	—	—	ZLOCK[2]	ZLOCK[1]	ZLOCK[0]

Table 23. PL_BF_ZCOMP Description

ZLOCK	Z-Lock Angle Threshold. Range is from 25° to 50°. Step size is 3.6°. Default value: **010** ≥ **32.1°**. Maximum value: **111** ≥ **50°**.
BKFR	Back Front Trip Angle Threshold. Default: 10 ≥ ±75°. Step size is 5°. Range: ±(65° to 80°).

Table 24. Back/Front Orientation Definitions

BKFR	Back → Front Transition	Front → Back Transition
00	Z < 80° or Z > 280°	Z > 100° and Z < 260°
01	Z < 75° or Z > 285°	Z > 105° and Z < 255°
10	Z < 70° or Z > 290°	Z > 110° and Z < 250°
11	Z < 65° or Z > 295°	Z > 115° and Z < 245°

0x1D - 0x1F: PL_P_L_THS_REG1, 2, 3 Portrait-to-Landscape Threshold Registers

The following registers represent the Portrait-to-Landscape trip threshold registers. These registers are used to set the trip angle for the image transition from the Portrait orientation to the Landscape orientation. The angle can be selected from Table 28 and the corresponding values for that angle should be written into the three PL_P_L_THS Registers.

0x1D PL_P_L_THS_REG1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P_L_THS[7]	P_L_THS[6]	P_L_THS[5]	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]

Table 25. PL_P_L_THS_REG1 Description

P_L_THS	Portrait-to-Landscape Threshold Register 1. Default value: **30°** → **0001_1010**.

0x1E PL_P_L_THS_REG2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P_L_THS[7]	P_L_THS[6]	P_L_THS[5]	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]

Table 26. PL_P_L_THS_REG2 Description

P_L_THS	Portrait-to-Landscape Threshold Register 2. Default value: **30°** → **0010_0010**.

0x1F PL_P_L_THS_REG3 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P_L_THS[7]	P_L_THS[6]	P_L_THS[5]	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]

Table 27. PL_P_L_THS_REG3 Description

P_L_THS	Portrait-to-Landscape Threshold Register 3. Default value: **30°**→ **1101_0100**.

Table 28. Portrait-to-Landscape Trip Angle Thresholds Look-up Table

Portrait-to-Landscape Trip Angle	PL_P_L_THS_REG1	PL_P_L_THS_REG2	PL_P_L_THS_REG3
15	0x17	0x75	0x77
20	0x18	0x14	0x23
25	0x18	0xF3	0x59
30	**0x1A**	**0x32**	**0xD5**
35	0x1B	0x92	0x77
40	0x1D	0x92	0x33
45	0x20	0x00	0x00
50	0x23	0x31	0xD9
55	0x27	0x71	0xB9
60	0x2D	0x41	0xA2

0x20 - 0x22 PL_L_P_THS_REG1, 2, 3 Landscape-to-Portrait Threshold Registers

The following registers represent the Landscape-to-Portrait trip threshold registers. These registers are used to set the trip angle for the image transition from the Landscape orientation to the Portrait orientation. The angle can be selected from Table 32 and the corresponding values for that angle should be written into the three PL_L_P_THS Registers.

0x20 PL_L_P_THS_REG1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L_P_THS[7]	L_P_THS[6]	L_P_THS[5]	L_P_THS[4]	L_P_THS[3]	L_P_THS[2]	L_P_THS[1]	L_P_THS[0]

Table 29. PL_L_P_THS_REG1 Description

L_P_THS	Landscape-to-Portrait Threshold Register 1. Default value: **60°** → **0010_1101**.

0x21 PL_L_P_THS_REG2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L_P_THS[7]	L_P_THS[6]	L_P_THS[5]	L_P_THS[4]	L_P_THS[3]	L_P_THS[2]	L_P_THS[1]	L_P_THS[0]

Table 30. PL_L_P_THS_REG2 Description

L_P_THS	Landscape-to-Portrait Threshold Register 2. Default value: **60°** → **0100_0001**.

0x22 PL_L_P_THS_REG3 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L_P_THS[7]	L_P_THS[6]	L_P_THS[5]	L_P_THS[4]	L_P_THS[3]	L_P_THS[2]	L_P_THS[1]	L_P_THS[0]

Table 31. PL_L_P_THS_REG3 Description

L_P_THS	Landscape-to-Portrait Threshold Register 3. Default value: **60°** → **1010_0010**.

Table 32. Landscape-to-Portrait Trip Angle Thresholds Look-up Table

Landscape-to-Portrait Trip Angle	PL_L_P_THS_REG1	PL_L_P_THS_REG2	PL_L_P_THS_REG3
30	0x1A	0x22	0xD4
35	0x1B	0x92	0x77
40	0x1D	0x92	0x33
45	0x20	0x00	0x00
50	0x23	0x31	0xD9

Table 32. Landscape-to-Portrait Trip Angle Thresholds Look-up Table

55	0x27	0x71	0xB9
60	**0x2D**	**0x41**	**0xA2**
65	0x35	0x91	0x8F
70	0x42	0x31	0x81
75	0x57	0x71	0x77

6.4 Freefall & Motion Detection Registers

For details on how to configure the device for Freefall and/or Motion detection and for sample code, refer to application note AN3917.

Note: There are two Freefall and Motion Detection Functions. The registers from 0x27 - 0x2A have the same descriptions as registers 0x23 - 0x26.

0x23: FF_MT_CFG_1 Freefall and Motion Configuration Register 1

0x23 FF_MT_CFG_1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ELE	OAE	ZHEFE	ZLEFE	YHEFE	YLEFE	XHEFE	XLEFE

Table 33. FF_MT_CFG_1 Description

ELE	Event Latch Enable: Event flag is latched into FF_MT_SRC_1 register. Reading of the FF_MT_SRC_1 register clears the EA event flag. Default value: 0 0: Event flag latch disabled; 1: Event flag latch enabled
OAE	Logical Or/And combination of events flags. Default value: 0 0: Logical AND combination of events flags; 1: Logical OR combination of events flags
ZHEFE	Event flag enable on Z High event. Default value: 0 0: Event detection disabled; 1: Event detection enabled
ZLEFE	Event flag enable on Z Low event. Default value: 0 0: Event detection disabled; 1: Event detection enabled
YHEFE	Event flag enable on Y High event. Default value: 0 0: Event detection disabled; 1: Event detection enabled
YLEFE	Event flag enable on Y Low event. Default value: 0 0: Event detection disabled; 1: Event detection enabled
XHEFE	Event flag enable on X High event. Default value: 0 0: Event detection disabled; 1: Event detection enabled
XLEFE	Event flag enable on X Low event. Default value: 0 0: Event detection disabled; 1: Event detection enabled

OAE bit allows the selection between Motion (logical OR combination of X, Y, Z-axis event flags) and Freefall (logical AND combination of X, Y, Z-axis event flags) detection.
ELE denotes whether the enabled event flag will be latched in the FF_MT_SRC_1 register or the event flag status in the FF_MT_SRC_1 will indicate the real-time status of the event. If ELE bit is set to a logic 1, then the event active “EA” flag is cleared by reading the FF_MT_SRC_1 source register.
ZHEFE, YHEFE, XHEFE enables the detection of a high g event when the measured acceleration data on X, Y, or Z-axis is higher than the threshold set in FF_MT_THS_1 register.
ZLEFE, YLEFE, XLEFE enables the detection of a low g event when the measured acceleration data on X, Y, or Z-axis is lower than the threshold set in FF_MT_THS_1 register.
FF_MT_THS_1 is the threshold register used by the Freefall/Motion function to detect Freefall or Motion events. The unsigned 7-bit FF_MT_THS_1 threshold register holds the threshold for the low g event detection where the magnitude of the X and Y and Z acceleration values are lower than the threshold value. Conversely the FF_MT_THS_1 also holds the threshold for the high g event detection where the magnitude of the X, or Y, or Z-axis acceleration values is higher than the threshold value.

0x24 FF_MT_SRC_1 Register

0x24: FF_MT_SRC_ Freefall and Motion Source Register (0x24) (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	EA	ZHE	ZLE	YHE	YLE	XHE	XLE

Table 34. FF_MT_SRC_1 Description

EA	Event Active Flag. Default value: 0 0: No event flag has been asserted; 1: one or more event flags have been asserted.
ZHE	Z High Event Flag. Default value: 0 0: No Z High event detected, 1: Z High event has been detected
ZLE	Z Low Event Flag. Default value: 0 0: No Z Low event detected, 1: Z Low event has been detected
YHE	Y High Event Flag. Default value: 0 0: No Y High event detected, 1: Y High event has been detected
YLE	Y Low Event Flag. Default value: 0 0: No Y Low event detected, 1: Y Low event has been detected
XHE	X High Event Flag. Default value: 0 0: No X High event detected, 1: X High event has been detected
XLE	X Low Event Flag. Default value: 0 0: No X Low event detected, 1: X Low event has been detected

This register keeps track of the acceleration event which is triggering (or has triggered, in case of ELE bit in FF_MT_CFG_1 register being set to 1) the event flag. In particular EA is set to a logic 1 when the logical combination of acceleration events flags specified in FF_MT_CFG_1 register is true. This bit is used in combination with the values in INT_EN_FF_MT_1 and INT_CFG_FF_MT_1 register to generate the Freefall/Motion interrupts.

An X,Y, or Z high or an X,Y, and Z high event is true when the acceleration value of the X or Y or Z axes is higher than the preset threshold value defined in the FF_MT_THS_1 register.

Conversely X,Y, or Z high or an X,Y, and Z low event is true when the acceleration value of the X and Y and Z axes are lower than the preset threshold value defined in the FF_MT_THS_1 register.

When the ELE bit is set, only the EA bit is latched. The other bits are not latched. To see the events that have been detected, the register must be read immediately. The EA bit will remain high until the source register is read.

0x25: FF_MT_THS_1 Freefall and Motion Threshold 1 Register

0x25 FF_MT_THS_1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 35. FF_MT_THS_1 Description

DBCNTM	Debounce counter mode selection. Default value: 0. 0: increments or decrements debounce, 1: increments or clears counter.
THS[6:0]	Freefall /Motion Threshold: default value: 000 0000

The minimum threshold resolution is dependent on the selected acceleration g range and the threshold register has a range of 0 to 127.
Therefore:

- If the selected acceleration g range is 8g mode (FS = 11), the minimum threshold resolution is 0.063g/LSB. The maximum value is 8g.
- If the selected acceleration g range is 4g mode (FS = 10), the minimum threshold resolution is 0.0315g/LSB. The maximum value is 4g.
- If the selected acceleration g range is 2g mode (FS = 01), the minimum threshold resolution is 0.01575g/LSB. The maximum value is 2g.

When DBCNTM bit is a logic '1', the debounce counter is cleared to 0 whenever the event of interest is no longer true (Figure 12 part b) while if the DBCNTM bit is set a logic '0' the debounce counter is decremented by 1 whenever the event of interest is no longer true (Figure 12 part c) until the debounce counter reaches 0 or the event of interest becomes active.

Decrementing of the debounce counter acts as a median filter enabling the system to filter out irregular spurious events which might impede the detection of the event.

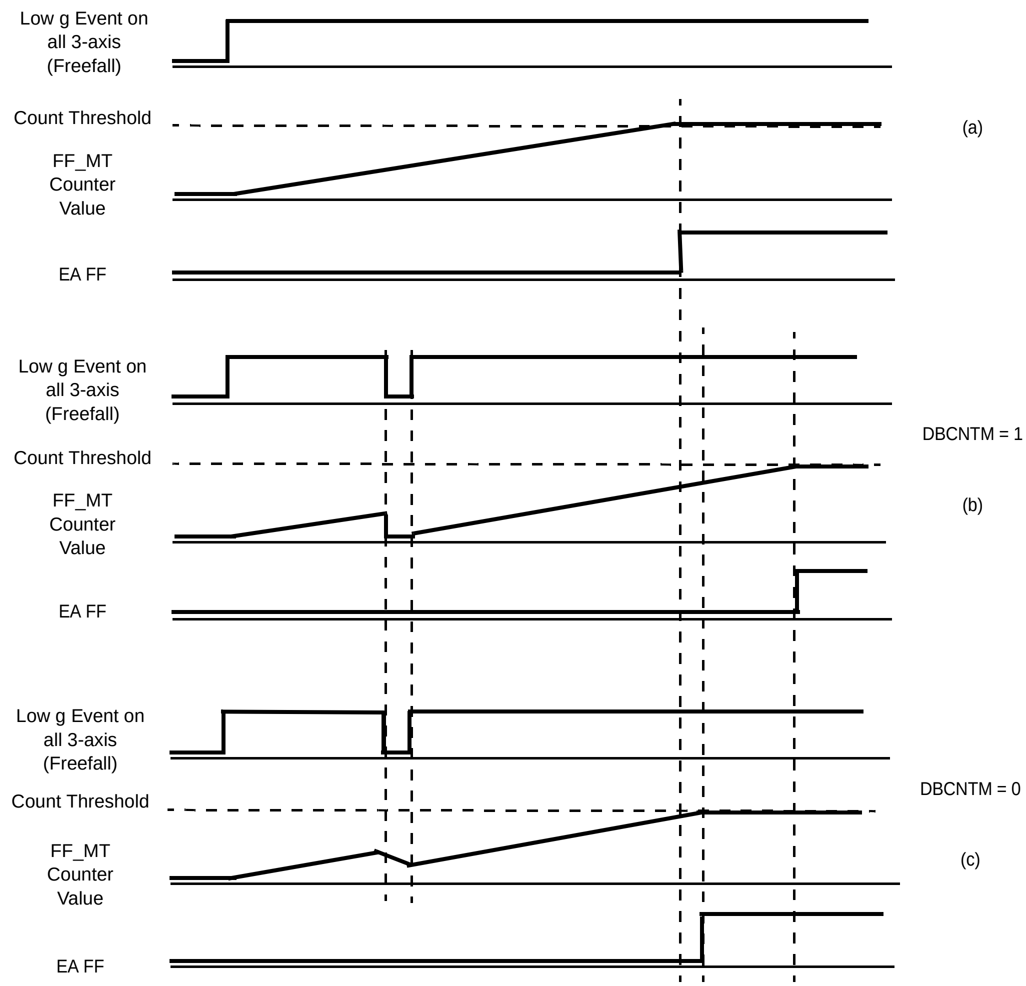


Figure 12. DBCNTM Bit Function

0x26: FF_MT_COUNT_1 Freefall Motion Count 1 Register

This register sets the number of debounce sample counts for the event trigger.

0x26 FF_MT_COUNT_1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 36. FF_MT_COUNT_1 Description

D[7-0]	Count value. Default value: 0000_0000

D7 - D0 define the number of debounce sample counts for the event trigger. When the debounce counter exceeds the FF_MT_COUNT_1 value, a Freefall/Motion event flag is set. The time step used for the debounce sample count depends on the ODR chosen (Table 37).

Table 37. FF_MT_COUNT_1 and FF_MT_COUNT_2 Relationship with the ODR

Output Data Rate (Hz)	Step	Duration Range
400	2.5 ms	2.5 ms – 0.63s
200	5 ms	5 ms – 1.275s
100	10 ms	10 ms – 2.55s
50	20 ms	20 ms – 5.1s
12.5	80 ms	80 ms – 20.4s
1.56	640 ms	640 ms – 163s

An ODR of 100 Hz and a FF_MT_COUNT_1 value of 15 would result in a debounce response time of 150 ms.

0x27: FF_MT_CFG_2 Freefall and Motion Configuration 2 Register

These registers all have the same descriptions as above for Registers 0x23 - 0x26.

0x27 FF_MT_CFG_2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ELE	OAE	ZHEFE	ZLEFE	YHEFE	YLEFE	XHEFE	XLEFE

0x28: FF_MT_SRC_2 Freefall and Motion Source 2 Register

0x28 FF_MT_SRC_2 Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	EA	ZHE	ZLE	YHE	YLE	XHE	XLE

0x29: FF_MT_THS_2 Freefall and Motion Threshold 2 Register

0x29 FF_MT_THS_2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

0x2A: FF_MT_COUNT_2 Freefall and Motion Debounce 2 Register

0x2A FF_MT_COUNT_2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

6.5 Transient Detection Registers

For more information on the uses of the transient function and sample code, refer to application note AN3918.

0x2B: TRANSIENT_CFG Transient Configuration Register

The transient detection mechanism can be configured to raise an interrupt when the magnitude of the high pass filtered data is greater than a user definable threshold. The TRANSIENT_CFG register is used to enable the transient interrupt generation mechanism for each of the 3 axes (X, Y, Z) of acceleration.

0x2B TRANSIENT_ CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	—	ELE	ZTEFE	YTEFE	XTEFE

Table 38. TRANSIENT_ CFG Description

ELE	Transient event flag is latched into the TRANSIENT_SRC register. Reading of the TRANSIENT_SRC register clears the event flag. Default value: 0 0: event flag latch disabled; 1: Event flag latch enabled
ZTEFE	Event flag enable on Z-axis. Default value: 0 0: Event detection disabled; 1: Event detection Enabled
YTEFE	Event flag enable on Y-axis. Default value: 0 0: Event detection disabled; 1: Event detection Enabled
XTEFE	Event flag enable on X-axis. Default value: 0 0: Event detection disabled; 1: Event detection Enabled

0x2C: TRANSIENT_SRC Transient Source Register

The transient source register is read to determine the source of an interrupt. When the ELE bit is set in Register0x2B the “EA” event Active bit in the source register is latched. The other bits in the source register are not latched. The source register must be read immediately following the interrupt to determine the axes the event occurred on. The interrupt for the transient event is cleared by reading the status register.

0x2C TRANSIENT_SRC Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	—	EA	ZTRANSE	YTRANSE	XTRANSE

Table 39. TRANSIENT_SRC Description

EA	Event Active Flag. Default value: 0 0: No event flag asserted; 1: one or more event flag has been asserted.
ZTRANSE	Z transient event. Default value: 0 0: No Z event detected, 1: Z event detected
YTRANSE	Y transient event. Default value: 0 0: No Y event detected, 1: Y event detected
XTRANSE	X transient event. Default value: 0 0: No X event detected, 1: X event detected

0x2D: TRANSIENT_THS Transient Threshold Register

The TRANSIENT_THS register sets the threshold limit for the high pass filtered acceleration. The value in the TRANSIENT_THS register corresponds to a g value which is compared against the values of OUT_X_DELTA, OUT_Y_DELTA, and OUT_Z_DELTA. If the acceleration exceeds the threshold limit an event flag is raised and an interrupt is generated if interrupts are enabled.

0x2D TRANSIENT_THS Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 40. TRANSIENT_THS Description

DBCNTM	Debounce counter mode selection. Default value: 0 0: increments or decrements debounce; 1: increments or clears counter
THS[6:0]	Transient Threshold: default value: 000_0000

The minimum threshold resolution is dependent on the selected acceleration g range and the threshold register has a range of 0 to 127.

Therefore:

- If the selected acceleration g range is 8g mode (FS = 11), the minimum threshold resolution is 0.063g/LSB. The maximum is 8g.
- If the selected acceleration g range is 4g mode (FS = 10), the minimum threshold resolution is 0.0315g/LSB. The maximum is 4g.
- If the selected acceleration g range is 2g mode (FS = 01), the minimum threshold resolution is 0.01575g/LSB. The maximum is 2g.
- The DBCNTM bit behaves in the same manner described previously for the Motion/Freefall 1.

0x2E: TRANSIENT_COUNT Transient Debounce Register

The TRANSIENT_COUNT sets the minimum number of debounce counts continuously matching the condition where the unsigned value of OUT_X_DELTA or OUT_Y_DELTA or OUT_Z_DELTA register is greater than the user specified value of TRANSIENT_THS.

0x2E TRANSIENT_COUNT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 41. TRANSIENT_COUNT Description

D[7-0]	Count value. Default value: 0000_0000

The time step for the Transient detection debounce counter is set by the value of the system ODR.

Table 42. TRANSIENT_COUNT relationship with the ODR

Output Data Rate (Hz)	Step	Duration Range
400	2.5 ms	2.5 ms – 0.637s
200	5 ms	5 ms – 1.275s
100	10 ms	10 ms – 2.55s
50	20 ms	20 ms – 5.1s
12.5	80 ms	80 ms – 20.4s
1.56	640 ms	640 ms – 163s

An ODR of 100 Hz and a TRANSIENT_COUNT value of 15 would result in a debounce response time of 150 ms.

6.6 Tap Detection Registers

For more details of how to configure the tap detection and sample code please refer to Freescale application note, AN3919. The tap detection registers are referred to as “Pulse”.

0x2F: PULSE_CFG Pulse Configuration Register

This register configures the event flag for the tap detection for enabling/disabling the detection of a single and double pulse on each of the axes.

0x2F PULSE_CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPA	ELE	ZDPEFE	ZSPEFE	YDPEFE	YSPEFE	XDPEFE	XSPEFE

Table 43. PULSE_CFG Description

DPA	Double Pulse Abort. 0: Double Pulse detection is not aborted if the start of a pulse is detected during the time period specified by the PULSE_LTCY register. 1: Setting the DPA bit momentarily suspends the double tap detection if the start of a pulse is detected during the time period specified by the PULSE_LTCY register and the pulse ends before the end of the time period specified by the PULSE_LTCY register.
ELE	Pulse event flags are latched into the PULSE_SRC register. Reading of the PULSE_SRC register clears the event flag. Default value: 0 0: Event flag latch disabled; 1: Event flag latch enabled
ZDPEFE	Event flag enable on double pulse event on Z-axis. Default value: 0 0: Event detection disabled; 1: Event detection enabled
ZSPEFE	Event flag enable on single pulse event on Z-axis. Default value: 0 0: Event detection disabled; 1: Event detection enabled
YDPEFE	Event flag enable on double pulse event on Y-axis. Default value: 0 0: Event detection disabled; 1: Event detection enabled
YSPEFE	Event flag enable on single pulse event on Y-axis. Default value: 0 0: Event detection disabled; 1: Event detection enabled
XDPEFE	Event flag enable on double pulse event on X-axis. Default value: 0 0: Event detection disabled; 1: Event detection enabled
XSPEFE	Event flag enable on single pulse event on X-axis. Default value: 0 0: Event detection disabled; 1: Event detection enabled

0x30: PULSE_SRC Pulse Source Register

This register indicates a double or single pulse event has occurred. The corresponding axis and event must be enabled in Register 0x2F for the event to be seen in the source register. The interrupt for the pulse event is cleared by reading the status register.

0x30 PULSE_SRC Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	EA	ZDPE	ZSPE	YDPE	YSPE	XDPE	XSPE

Table 44. TPULSE_SRC Description

EA	Event Active Flag. Default value: 0 0: no event flag has been asserted; 1: one or more events have been asserted
ZDPE	Double pulse on Z-axis event. Default value: 0 0: no event detected; 1: Double Z event detected
ZSPE	Single pulse on Z-axis event. Default value: 0 0: no event detected; 1: Single Z event detected
YDPE	Double pulse on Y-axis event. Default value: 0 0: no event detected; 1: Double Y event detected
YSPE	Single pulse on Y-axis event. Default value: 0 0: no event detected; 1: Single Y event detected
XDPE	Double pulse on X-axis event. Default value: 0 0: no event detected; 1: Double X event detected
XSPE	Single pulse on X-axis event. Default value: 0 0: no event detected; 1: Single X event detected

0x31 - 0x33: PULSE_THSX, Y, Z Pulse Threshold for X, Y & Z Registers

The pulse threshold can be set separately for the X, Y and Z axes. The threshold values range from 0 to 31 counts with steps of 0.258g/LSB **at a fixed 8g acceleration range**, thus the minimum resolution is always fixed at 0.258g/LSB irrespective of the selected g range.

The PULSE_THSX, PULSE_THSY and PULSE_THSZ registers define the threshold which is used by the system to start the pulse detection procedure. The threshold value is expressed over 5-bits as an unsigned number.

0x31 PULSE_THSX Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	THSX4	THSX3	THSX2	THSX1	THSX0

Table 45. PULSE_THSX Description

THSX4, THSX0	Pulse Threshold on X-axis. Default value: 0_0000

0x32 PULSE_THSY Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	THSY4	THSY3	THSY2	THSY1	THSY0

Table 46. PULSE_THSY Description

THSY4, THSY0	Pulse Threshold on Y-axis. Default value: 0_0000

0x33 PULSE_THSZ Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 47. PULSE_THSZ Description

THSZ4, THSZ0	Pulse Threshold on Z-axis. Default value: 0_0000

0x34: PULSE_TMLT Pulse Time Window 1 Register

0x34 PULSE_TMLT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tmlt7	Tmlt6	Tmlt5	Tmlt4	Tmlt3	Tmlt2	Tmlt1	Tmlt0

The bits Tmlt7 through Tmlt0 define the maximum time interval that can elapse between the start of the acceleration on the selected axis exceeding the specified threshold and the end when the acceleration on the selected axis must go below the specified threshold to be considered a valid pulse.

The minimum time step for the pulse time limit is defined in Table 48. Maximum time for a given ODR is the minimum time step at the given power mode multiplied by 255. The time steps available are dependent on whether the device is in Normal Power mode or in Low Power mode. Notice in the table below that the time step is twice as long in Low Power mode.

Table 48. Time Step for PULSE Time Limit at ODR and Power Mode

Output Data Rate (Hz)	Step at Normal Mode	Step at Low Power Mode
400	0.625 ms	1.25 ms
200	1.25 ms	2.5 ms
100	2.5 ms	5.0 ms
50	5 ms	10 ms
12.5	5 ms	10 ms
1.56	5 ms	10 ms

Therefore an ODR setting of 400 Hz with normal power mode would result in a maximum pulse time limit of (0.625 ms * 255) ≥ 159 ms.

0x35: PULSE_LTCY Pulse Latency Timer Register

0x35 PULSE_LTCY Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ltcy7	Ltcy6	Ltcy5	Ltcy4	Ltcy3	Ltcy2	Ltcy1	Ltcy0

The bits Ltcy7 through Ltcy0 define the time interval that starts after the first pulse detection. During this time interval, all pulses are ignored. **Note:** This timer must be set for single pulse and for double pulse.

The minimum time step for the pulse latency is defined in Table 49. The maximum time is the time step at the ODR and Power Mode multiplied by 255. Notice that the time step is twice the duration if the device is operating in Low Power mode, as shown below.

Table 49. Time Step for PULSE Latency at ODR and Power Mode

Output Data Rate (Hz)	Step at Normal Mode	Step at Low Power Mode
400	1.25 ms	2.5 ms
200	2.5 ms	5.0 ms
100	5.0 ms	20 ms
50	10 ms	20 ms
12.5	10 ms	20 ms
1.56	10 ms	20 ms

0x36: PULSE_WIND Second Pulse Time Window Register

0x36 PULSE_WIND Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Wind7	Wind6	Wind5	Wind4	Wind3	Wind2	Wind1	Wind0

The bits Wind7 through Wind0 define the maximum interval of time that can elapse after the end of the latency interval in which the start of the second pulse event must be detected provided the device has been configured for double pulse detection. The detected second pulse width must be shorter than the time limit constraints specified by the PULSE_TMLT register, but the end of the double pulse need not finish within the time specified by the PULSE_WIND register.

The minimum time step for the pulse window is defined in Table 50. The maximum time is the time step at the ODR and Power Mode multiplied by 255.

Table 50. Time Step for PULSE Detection Window at ODR and Power Mode

Output Data Rate (Hz)	Step at Normal Mode	Step at Low Power Mode
400	1.25 ms	2.5 ms
200	2.5 ms	5.0 ms
100	5.0 ms	20 ms
50	10 ms	20 ms
12.5	10 ms	20 ms
1.56	10 ms	20 ms

6.7 Auto-Sleep Registers

For additional information on how to configure the device for the Auto-Sleep/Wake feature, refer to AN3921.

0x37: ASLP_COUNT Auto-Sleep Inactivity Timer Register

The ASLP_COUNT register sets the minimum time period of inactivity required to change current ODR value from the value specified in the **DR[2:0]** to **ASLP_RATE** (Reg 0x38) value provided the **SLPE** bit is set to a logic ‘1’ in the **CTRL_REG2** register.

0x37 ASLP_COUNT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 51. ASLP_COUNT Description

D[7-0]	Duration value. Default value: 0000 0000

D7-D0 defines the minimum duration time to change current ODR value from **DR** to **ASLP_RATE**. Time step and maximum value depend on the ODR chosen (see Table 52).

Table 52. ASLP_COUNT Relationship with ODR

Output Data Rate (ODR)	Duration	Step
400	0 to 81s	320 ms
200	0 to 81s	320 ms
100	0 to 81s	320 ms
50	0 to 81s	320 ms
12.5	0 to 81s	320 ms
1.56	0 to 162s	640 ms

In order to wake the device, the desired function or functions must be enabled and set to “Wake From Sleep”. All enabled functions will still function in sleep mode at the sleep ODR. Only the functions that have been selected for “Wake From Sleep” will **wake** the device.

MMA8450Q has 6 functions that can be used to keep the sensor from falling asleep namely, Transient, Orientation, Tap, Motion/FF1 and Motion/FF2 and the FIFO. One or more of these functions can be enabled. In order to wake the device, functions are provided namely, Transient, Orientation, Tap, and the two Motion/Freefall. Note that the FIFO does not wake the device. The Auto-Wake/Sleep interrupt does not affect the wake/sleep, nor does the data ready interrupt. The FIFO gate (bit 7) in Register 0x3A, when set, will hold the last data in the FIFO before transitioning to a different ODR. After the buffer is flushed, it will accept new sample data at the current ODR. See Register 0x3A for the wake from sleep bits.

If the Auto-Sleep bit is disabled, then the device can only toggle between Standby and Wake Mode by writing to the FS0 and FS1 bits in Register 0x38 Ctrl Reg1. If Auto-Sleep interrupt is enabled, transitioning from Active mode to Auto-Sleep mode and vice versa generates an interrupt.

0x38: CTRL_REG1 System Control 1 Register

0x38 CTRL_REG1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASLP_RATE1	ASLP_RATE0	0	DR2	DR1	DR0	FS1	FS0

Table 53. CTRL_REG1 Description

ASLP_RATE [1:0]	This register configures the Auto-Wake sample frequency when the device is in Sleep Mode. See Table 54 for more information.
DR[2:0]	Data rate selection. Default value: 000
FS[1:0]	Full Scale selection. Default value: 00 (00: Standby mode; 01: active mode ±2g; 10: active mode ±4g; 11: active mode ±8g)

Table 54. Sleep Mode Poll Rate Description

ASLP_RATE1	ASLP_RATE0	Frequency (Hz)
0	0	50
0	1	25
1	0	12.5
1	1	1.56

It is important to note that when the device is in Auto-Sleep mode, the system ODR and the data rate for all the system functional blocks are overwritten by the data rate set by the **ASLP_RATE** field in Register 0x38.

DR[2:0] bits select the output data rate (ODR) for acceleration samples. The default value is 000 for a data rate of 400 Hz.

Table 55. System Output Data Rate Selection

DR2	DR1	DR0	Output Data Rate (ODR)	Time Between Data Samples
0	0	0	400 Hz	2.5 ms
0	0	1	200 Hz	5 ms

Table 55. System Output Data Rate Selection

0	1	0	100 Hz	10 ms
0	1	1	50 Hz	20 ms
1	0	0	12.5 Hz	80 ms
1	0	1	1.563 Hz	640 ms

FS[1:0] bits select between standby mode and active mode. The default value is 00 for standby mode.

Table 56. Full Scale Selection

FS1	FS0	Mode	g Range
0	0	Standby	—
0	1	Active	±2g
1	0	Active	±4g
1	1	Active	±8g

0x39: CTRL_REG2 System Control 2 Register

0x39 CTRL_REG2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ST	BOOT	0	0	0	0	SLPE	MODS

Table 57. CTRL_REG2 Description

ST	Self-Test Enable. Default value: 0 0: Self-Test disabled; 1: Self-Test enabled
BOOT	Reboot device content (Software Reset). Default value: 0 0: device reboot disabled; 1: device reboot enabled.
SLPE(1)	Auto-Sleep enable. Default value: 0 0: Auto-Sleep is not enabled; 1: Auto-Sleep is enabled.
MODS	Low power mode / Normal mode selection. Default value: 0 0: normal mode; 1: low power mode.

1. When SLPE = 1, the transitioning between sleep mode and wake mode results in a FIFO flush and a reset of internal functional block counters. All functional block status information are preserve except otherwise stated. See Table 58 for more information about the FIFO_GATE bit in CTRL_REG3 register.

ST bit activates the Self-Test function. When ST is set to one, an output change will occur to the device outputs (refer to Table 2 and Table 3) thus allowing host application to check the functionality of the entire signal chain.

BOOT bit is used to activate the software reset. The Boot mechanism can be enabled in STANDBY and ACTIVE mode.

When the Boot bit is enabled the Boot mechanism resets all functional block registers and loads the respective internal registers with default NVM values.

The system will automatically transition to standby mode if not already in standby mode before the software reset (re-BOOT process) can occur.

Note: The I^2C communication system is reset to avoid accidental corrupted data access.

0x3A: CTRL_REG3 Interrupt Control Register

0x3A CTRL_REG3 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT_1	WAKE_FF_MT_2	IPOL	PP_OD

Table 58. CTRL_REG3 Description

FIFO_GATE	0: FIFO gate is bypassed. FIFO is flushed upon the system mode transitioning from wake-to-sleep mode or from sleep-to-wake mode. 1: The FIFO input buffer is blocked when transitioning from “wake-to-sleep” mode or from “sleep-to-wake” mode until the FIFO is flushed. Although the system transitions from “wake-to-sleep” or from “sleep-to-wake” the contents of the FIFO buffer are preserved, new data samples are ignored until the FIFO is emptied by the host application. If the FIFO_GATE bit is set to logic 1 and the FIFO buffer is not emptied before the arrival of the next sample, then the FGERR bit in the SYS_MOD register (0x14) will be asserted. The FGERR bit remains asserted as long as the FIFO buffer remains un-emptied. Emptying the FIFO buffer clears the FGERR bit in the SYS_MOD register.
WAKE_TRANS	0: Transient function is bypassed in sleep mode 1: Transient function interrupt can wake up system
WAKE_LNDPRT	0: Orientation function is bypassed in sleep mode 1: Orientation function interrupt can wake up system
WAKE_PULSE	0: Pulse function is bypassed in sleep mode 1: Pulse function interrupt can wake up system
WAKE_FF_MT_1	0: Freefall/Motion1 function is bypassed in sleep mode 1: Freefall/Motion1 function interrupt can wake up
WAKE_FF_MT_2	0: Freefall/Motion2 function is bypassed in sleep mode 1: Freefall/Motion2 function interrupt can wake up system
IPOL	Interrupt polarity active high, or active low. Default value 0. 0: active low; 1: active high
PP_OD	Push-pull/Open Drain selection on interrupt pad. Default value 0. 0: push-pull; 1: open drain

IPOL bit selects the polarity of the interrupt signal. When IPOL is ‘0’ any interrupt event will signalled with a logical 0.
PP_OD bit configures the interrupt pin to Push-Pull or in Open Drain mode. The open drain configuration can be used for connecting multiple interrupt signals on the same interrupt line.

0x3C: CTRL_REG5 Register (Read/Write)

0x3C CTRL_REG5 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPRT	INT_EN_PULSE	INT_EN_FF_MT_1	INT_EN_FF_MT_2	INT_EN_DRDY

Table 59. interrupt Enable Register Description

Interrupt Enable	Description
INT_EN_ASLP	Interrupt Enable. Default value: 0 0: Auto-Sleep/Wake interrupt disabled; 1: Auto-Sleep/Wake interrupt enabled.
INT_EN_FIFO	Interrupt Enable. Default value: 0 0: FIFO interrupt disabled; 1: FIFO interrupt enabled.
INT_EN_TRANS	Interrupt Enable. Default value: 0 0: Transient interrupt disabled; 1: Transient interrupt enabled.
INT_EN_LNDPRT	Interrupt Enable. Default value: 0 0: Orientation (Landscape/Portrait) interrupt disabled. 1: Orientation (Landscape/Portrait) interrupt enabled.
INT_EN_PULSE	Interrupt Enable. Default value: 0 0: Pulse Detection interrupt disabled; 1: Pulse Detection interrupt enabled
INT_EN_FF_MT_1	Interrupt Enable. Default value: 0 0: Freefall/Motion1 interrupt disabled; 1: Freefall/Motion1 interrupt enabled
INT_EN_FF_MT_2	Interrupt Enable. Default value: 0 0: Freefall/Motion2 interrupt disabled; 1: Freefall/Motion2 interrupt enabled
INT_EN_DRDY	Interrupt Enable. Default value: 0 0: Data Ready interrupt disabled; 1: Data Ready interrupt enabled

The corresponding functional block interrupt enable bit allows the functional block to route its event detection flags to the system's interrupt controller. The interrupt controller routes the enabled functional block interrupt to the INT1 or INT2 pin.

0x3C: CTRL_REG5 Interrupt Configuration Register

0x3C CTRL_REG5 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT_1	INT_CFG_FF_MT_2	INT_CFG_DRDY

Table 60. Interrupt Configuration Register Description

Interrupt Configuration	Description
INT_CFG_ASLP	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_FIFO	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_TRANS	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_LNDPRT	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_PULSE	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_FF_MT_1	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_FF_MT_2	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_DRDY	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin

The system's interrupt controller shown in Figure 10 uses the corresponding bit field in the CTRL_REG5 register to determine the routing table for the INT1 and INT2 interrupt pins. If the bit value is logic '0' the functional block's interrupt is routed to INT2, and if the bit value is logic '1' then the interrupt is routed to INT1. One or more functions can assert an interrupt pin; therefore a host application responding to an interrupt should read the INT_SOURCE (0x15) register to determine the appropriate sources of the interrupt.

6.8 User Offset Correction Registers

For more information on how to calibrate the 0g Offset refer to AN3916 Offset Calibration Using the MMA8450Q. The 2's complement offset correction registers values are used to realign the zero g position of the X, Y, and Z-axis after device board mount. The resolution of the offset registers is 3.906 mg per LSB. The 2's complement 8-bit value would result in an offset compensation range ±0.5g.

0x3D: OFF_X Offset Correction X Register

0x3D OFF_X Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 61. OFF_X Description

D7-D0	X -axis offset trim LSB value. Default value: 0000_0000.

0x3E: OFF_Y Offset Correction Y Register

0x3E OFF_Y Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 62. OFF_Y Description

D7-D0	Y-axis offset trim LSB value. Default value: 0000_0000.

0x3F: OFF_Z Offset Correction Z Register

0x3F OFF_Z Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 63. OFF_Z Description

D7-D0	Z-axis offset trim LSB value. Default value: 0000_0000.

Appendix A

Table 64. MMA8450Q Register Map

Reg	Name	Definition	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	STATUS	Data Status R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
01	OUT_X_MSB	8-bit X Data R	XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4
02	OUT_Y_MSB	8-bit Y Data R	YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4
03	OUT_Z_MSB	8-bit Z Data R	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4
04	STATUS	Data Status R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
05	OUT_X_LSB	12-bit X Data R	0	0	0	0	XD3	XD2	XD1	XD0
06	OUT_X_MSB	12-bit X Data R	XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4
07	OUT_Y_LSB	12-bit Y Data R	0	0	0	0	YD3	YD2	YD1	YD0
08	OUT_Y_MSB	12-bit Y Data R	YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4
09	OUT_Z_LSB	12-bit Z Data R	0	0	0	0	ZD3	ZD2	ZD1	ZD0
0A	OUT_Z_MSB	12-bit Z Data R	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4
0B	STATUS	Data Status R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
0C	OUT_X_DELTA	8-bit Transient X Data R	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
0D	OUT_Y_DELTA	8-bit Transient Y Data R	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
0E	OUT_Z_DELTA	8-bit Transient Z Data R	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
0F	WHO_AM_I	ID Register R	—	—	—	—	—	—	—	—
10	F_STATUS	FIFO Status R	F_OVF	F_WMRK_FLAG	F_CNT5	F_CNT4	F_CNT3	F_CNT2	F_CNT1	F_CNT0
11	F_8DATA	8-bit FIFO Data R	XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4
12	F_12DATA	12-bit FIFO Data R	0	0	0	0	XD3	XD2	XD1	XD0
13	F_SETUP	FIFO Setup R/W	F_MODE1	F_MODE0	F_WMRK5	F_WMRK4	F_WMRK3	F_WMRK2	F_WMRK1	F_WMRK0
14	SYSMOD	System Mode R	PERR	FGERR	0	0	0	0	SYSMOD1	SYSMOD0
15	INT_SOURCE	Interrupt Status R	SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT_1	SRC_FF_MT_2	SRC_DRDY
16	XYZ_DATA_CFG	Data Config. R/W	FDE	0	0	0	—	ZDEFE	YDEFE	XDEFE
17	HP_FILTER_CUTOFF	HP Filter Setting R/W	0	0	0	0	0	0	SEL1	SEL0
18	PL_STATUS	PL Status R	NEWLP	LO	-	LAPO[2]	LAPO[1]	LAPO[0]	BAFRO[1]	BAFRO[0]
19	PL_PRE_STATUS	Previous PL Status R	-	LO	-	LAPO[2]	LAPO[1]	LAPO[0]	BAFRO[1]	BAFRO[0]
1A	PL_CFG	PL Configuration R/W	DBCNTM	PL_EN	-	-	-	GOFF[2]	GOFF[1]	GOFF[0]
1B	PL_COUNT	PL Debounce R/W	DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE [2]	DBNCE [1]	DBNCE [0]
1C	PL_BF_ZCOMP	PL Back/Front and Z Compensation R/W	BKFR[1]	BKFR[0]	-	-	-	ZLOCK[2]	ZLOCK[1]	ZLOCK[0]
1D	PL_P_L_THS_REG1	Portrait-to-Landscape Threshold Setting 1 R/W	P_L_THS[7]	P_L_THS[6]	P_L_THS[5]	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]
1E	PL_P_L_THS_REG2	Portrait-to-Landscape Threshold Setting 2 R/W	P_L_THS[7]	P_L_THS[6]	P_L_THS[5]	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]
1F	PL_P_L_THS_REG3	Portrait-to-Landscape Threshold Setting 3 R/W	P_L_THS[7]	P_L_THS[6]	P_L_THS[5]	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]
20	PL_L_P_THS_REG1	Landscape-to-Portrait Threshold Setting 1 R/W	L_P_THS[7]	L_P_THS[6]	L_P_THS[5]	L_P_THS[4]	L_P_THS[3]	L_P_THS[2]	L_P_THS[1]	L_P_THS[0]
21	PL_L_P_THS_REG2	Landscape-to-Portrait Threshold Setting21 R/W	L_P_THS[7]	L_P_THS[6]	L_P_THS[5]	L_P_THS[4]	L_P_THS[3]	L_P_THS[2]	L_P_THS[1]	L_P_THS[0]
22	PL_L_P_THS_REG3	Landscape-to-Portrait Threshold Setting 3 R/W	L_P_THS[7]	L_P_THS[6]	L_P_THS[5]	L_P_THS[4]	L_P_THS[3]	L_P_THS[2]	L_P_THS[1]	L_P_THS[0]
23	FF_MT_CFG_1	FF/Motion Config. 1 R/W	ELE	OAE	ZHEFE	ZLEFE	YHEFE	YLEFE	XHEFE	XLEFE
24	FF_MT_SRC_1	FF/Motion Source 1 R	—	EA	ZHE	ZLE	YHE	YLE	XHE	XLE
25	FF_MT_THS_1	FF/Motion Threshold 1 R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
26	FF_MT_COUNT_1	FF/Motion Debounce 1 R/W	D7	D6	D5	D4	D3	D2	D1	D0
27	FF_MT_CFG_2	FF/Motion Config. 2 R/W	ELE	OAE	ZHEFE	ZLEFE	YHEFE	YLEFE	XHEFE	XLEFE
28	FF_MT_SRC_2	FF/Motion Source 2 R	—	EA	ZHE	ZLE	YHE	YLE	XHE	XLE

Table 64. MMA8450Q Register Map

29	FF_MT_THS_2	FF/Motion Threshold 2 R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
2A	FF_MT_COUNT_2	FF/Motion Debounce 2 R/W	D7	D6	D5	D4	D3	D2	D1	D0
2B	TRANSIENT_CFG	Transient Config. R/W	—	—	—	—	ELE	ZTEFE	YTEFE	XTEFE
2C	TRANSIENT_SRC	Transient Source R	—	—	—	—	EA	ZTRANSE	YTRANSE	XTRANSE
2D	TRANSIENT_THS	Transient Threshold R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
2E	TRANSIENT_COUNT	Transient Debounce R/W	D7	D6	D5	D4	D3	D2	D1	D0
2F	PULSE_CFG	Pulse Config. R/W	DPA	ELE	ZDPEFE	ZSPEFE	YDPEFE	YSPEFE	XDPEFE	XSPEFE
30	PULSE_SRC	Pulse Source R	—	EA	ZDPE	ZSPE	YDPE	YSPE	XDPE	XSPE
31	PULSE_THSX	Pulse X Threshold R/W	0	0	0	THSX4	THSX3	THSX2	THSX1	THSX0
32	PULSE_THSY	Pulse Y Threshold R/W	0	0	0	THSY4	THSY3	THSY2	THSY1	THSY0
33	PULSE_THSZ	Pulse Z Threshold R/W	0	0	0	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
34	PULSE_TMLT	Pulse First Timer R/W	Tmlt7	Tmlt6	Tmlt5	Tmlt4	Tmlt3	Tmlt2	Tmlt1	Tmlt0
35	PULSE_LTCY	Pulse Latency R/W	Ltcy7	Ltcy6	Ltcy5	Ltcy4	Ltcy3	Ltcy2	Ltcy1	Ltcy0
36	PULSE_WIND	Pulse 2nd Window R/W	Wind7	Wind6	Wind5	Wind4	Wind3	Wind2	Wind1	Wind0
37	ASLP_COUNT	Auto-Sleep Counter R/W	D7	D6	D5	D4	D3	D2	D1	D0
38	CTRL_REG1	Control Reg 1 R/W	ASLP_RATE1	ASLP_RATE0	0	DR2	DR1	DR0	FS1	FS0
39	CTRL_REG2	Control Reg 2 R/W	ST	RST	0	0	0	0	SLPE	MODS
3A	CTRL_REG3	Control Reg3 R/W (Wake Interrupts from Sleep)	FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT_1	WAKE_FF_MT_2	IPOL	PP_OD
3B	CTRL_REG4	Control Reg4 R/W (Interrupt Enable Map)	INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPRT	INT_EN_PULSE	INT_EN_FF_MT_1	INT_EN_FF_MT_2	INT_EN_DRDY
3C	CTRL_REG5	Control reg5 R/W (Interrupt Configuration)	INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT_1	INT_CFG_FF_MT_2	INT_CFG_DRDY
3D	OFF_X	X 8-bit offset	D7	D6	D5	D4	D3	D2	D1	D0
3E	OFF_Y	Y 8-bit offset	D7	D6	D5	D4	D3	D2	D1	D0
3F	OFF_Z	Z 8-bit offset	D7	D6	D5	D4	D3	D2	D1	D0

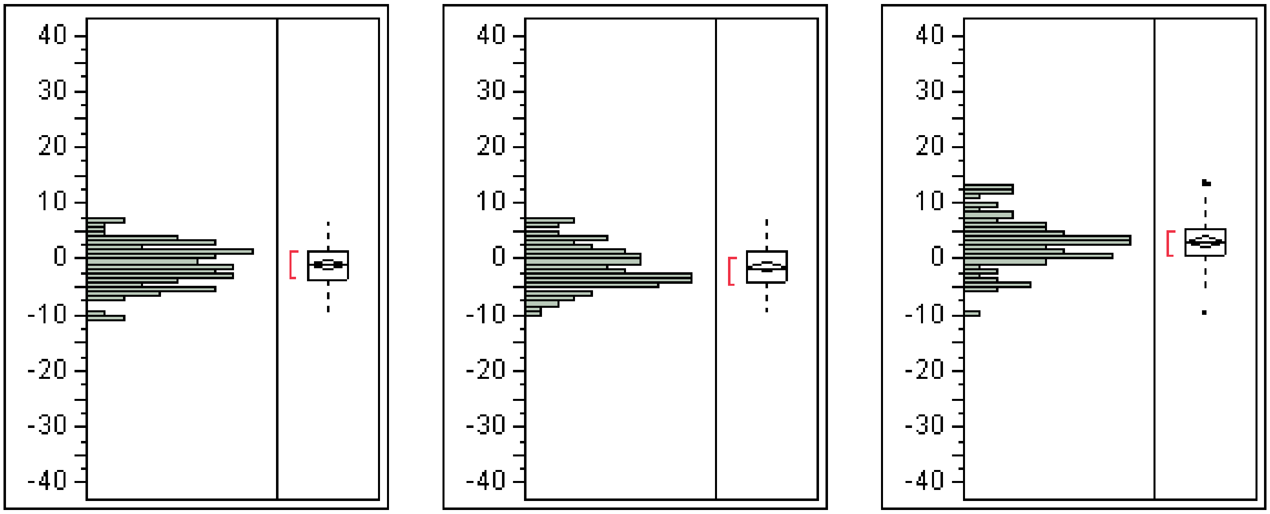
Table 65. Accelerometer Output Data

12-bit Data	Range ±2g	Range ±4g	Range ±8g
0111 1111 1111	1.999g	+3.998g	+7.996g
0111 1111 1110	1.998g	+3.996g	+7.992g
—	—	—	—
0000 0000 0001	0.001g	+0.002g	+0.004g
0000 0000 0000	0.000g	0.000g	0.000g
1111 1111 1111	-0.001g	-0.002g	-0.004g
—	—	—	—
1000 0000 0001	-1.999g	-3.998g	-7.996g
1000 0000 0000	-2.000g	-4.000g	-8.000g
8- bit Data	Range ±2g	Range ±4g	Range ±8g
0111 1111	1.984g	+3.968g	+7.936g
0111 1110	1.968g	+3.936g	+7.872g
—	—	—	—
0000 0001	+0.016g	+0.032g	+0.064g
0000 0000	0.000g	0.000g	0.000g
1111 1111	-0.016g	-0.032g	-0.064g
—	—	—	—
1000 0001	-1.984g	-3.968g	-7.936g
1000 0000	-2.000g	-4.000g	-8.000g

Appendix B

Distributions

Initial X 0g Offset	Initial Y 0g Offset	Initial Z 0g Offset



Quantiles

	Initial X 0g Offset	Initial Y 0g Offset	Initial Z 0g Offset
100.0% maximum	7.03	7.486	13.15
99.5%	7.03	7.486	13.15
97.5%	6.90	6.869	12.96
90.0%	3.58	3.667	9.50
75.0% quartile	1.34	1.290	5.37
50.0% median	-1.02	-1.806	3.00
25.0% quartile	-3.63	-4.028	0.43
10.0%	-5.97	-6.444	-3.40
2.5%	-10.07	-8.699	-5.54
0.5%	-10.43	-9.621	-9.95
0.0% minimum	-10.43	-9.621	-9.95

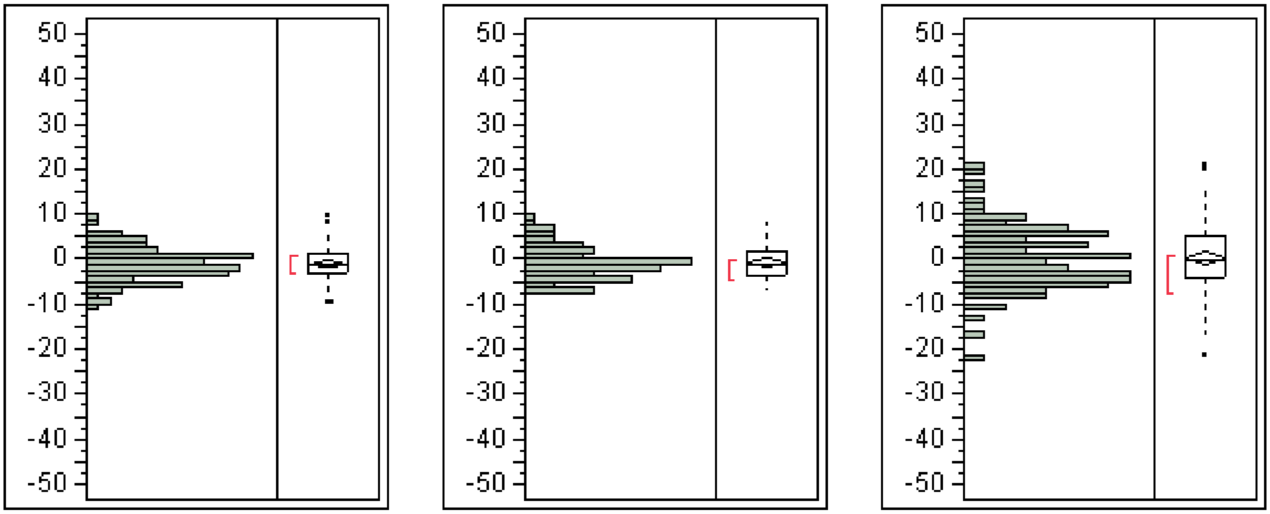
Moments

	Initial X 0g Offset	Initial Y 0g Offset	Initial Z 0g Offset
Mean	-1.137584	-1.318382	3.0432135
Std Dev	3.7502043	3.7963513	4.586924
Std Err Mean	0.3975209	0.4024124	0.486213
Upper 95% Mean	-0.347595	-0.518672	4.0094596
Lower 95% Mean	-1.927573	-2.118092	2.0769674
N	89	89	89

Figure 13. Distribution of Pre Board Mounted Devices Tested in Sockets (1 count = 3.9 mg)

Distributions

Post BM X 0g Offset	Post BM Y 0g Offset	Post BM Z 0g Offset



Quantiles

Post BM X 0g Offset	100.0%	maximum	8.92
	99.5%		8.92
	97.5%		7.20
	90.0%		4.44
	75.0%	quartile	1.11
	50.0%	median	-1.24
	25.0%	quartile	-3.18
	10.0%		-5.98
	2.5%		-9.74
	0.5%		-10.03
	0.0%	minimum	-10.03
Post BM Y 0g Offset	100.0%	maximum	8.842
	99.5%		8.842
	97.5%		7.715
	90.0%		4.921
	75.0%	quartile	1.774
	50.0%	median	-1.067
	25.0%	quartile	-3.509
	10.0%		-5.611
	2.5%		-7.000
	0.5%		-7.061
	0.0%	minimum	-7.061
Post BM Z 0g Offset	100.0%	maximum	20.41
	99.5%		20.41
	97.5%		18.73
	90.0%		9.43
	75.0%	quartile	5.06
	50.0%	median	-0.29
	25.0%	quartile	-4.26
	10.0%		-7.51
	2.5%		-16.14
	0.5%		-21.74
	0.0%	minimum	-21.74

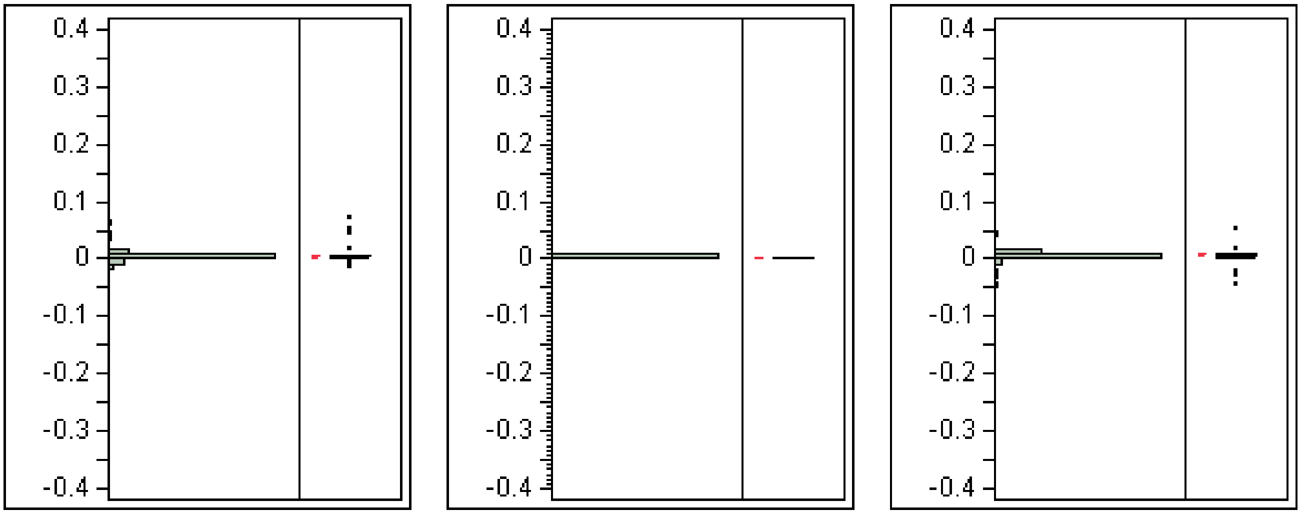
Moments

	Post BM X 0g Offset	Post BM Y 0g Offset	Post BM Z 0g Offset
Mean	-1.055764	-0.779056	0.2342135
Std Dev	3.8134703	3.7638495	7.3810254
Std Err Mean	0.404227	0.3989673	0.7823871
Upper 95% Mean	-0.252448	0.0138074	1.7890435
Lower 95% Mean	-1.85908	-1.57192	-1.320617
N	89	89	89

Figure 14. Distribution of Post Board Mounted Devices (1 count = 3.9 mg)

Distributions

		%/C X Axis Sense -40C	%/C X Axis Sense 25C	%/C X Axis Sense 85C



Quantiles

		%/C X Axis Sense -40C	%/C X Axis Sense 25C	%/C X Axis Sense 85C
100.0%	maximum	0.0658	0	0.0498
99.5%		0.0658	0	0.0498
97.5%		0.0399	0	0.0131
90.0%		0.0084	0	0.0103
75.0%	quartile	0.0064	0	0.0081
50.0%	median	0.0040	0	0.0057
25.0%	quartile	0.0018	0	0.0033
10.0%		-4.6e-5	0	0.0018
2.5%		-0.0064	0	-0.0253
0.5%		-0.0160	0	-0.0486
0.0%	minimum	-0.0160	0	-0.0486

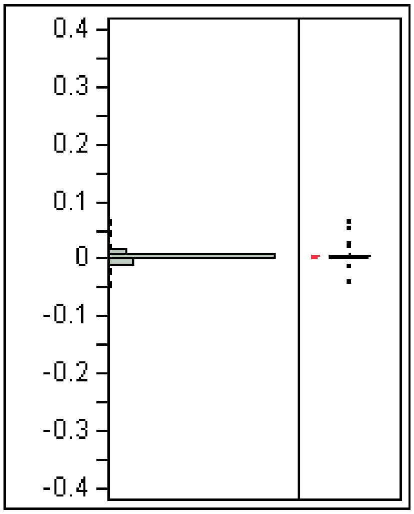
Moments

	%/C X Axis Sense -40C	%/C X Axis Sense 25C	%/C X Axis Sense 85C
Mean	0.005049	0	0.0052493
Std Dev	0.0086028	0	0.0085428
Std Err Mean	0.0007987	0	0.0007932
Upper 95% Mean	0.0066312	0	0.0068205
Lower 95% Mean	0.0034668	0	0.0036782
N	116	116	116

Figure 15. 2g/4g/8g X-axis TCS (%/°C)

Distributions

%/C Y Axis Sense -40C



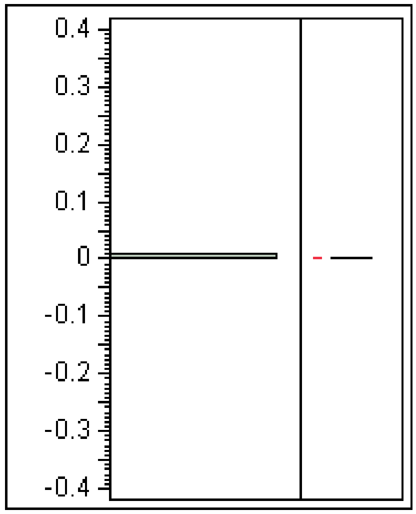
Quantiles

100.0%	maximum	0.0592
99.5%		0.0592
97.5%		0.0231
90.0%		0.0087
75.0%	quartile	0.0062
50.0%	median	0.0039
25.0%	quartile	0.0015
10.0%		-0.0009
2.5%		-0.0050
0.5%		-0.0450
0.0%	minimum	-0.0450

Moments

Mean	0.0042506
Std Dev	0.0090969
Std Err Mean	0.0008483
Upper 95% Mean	0.0059311
Lower 95% Mean	0.0025701
N	115

%/C Y Axis Sense 25C



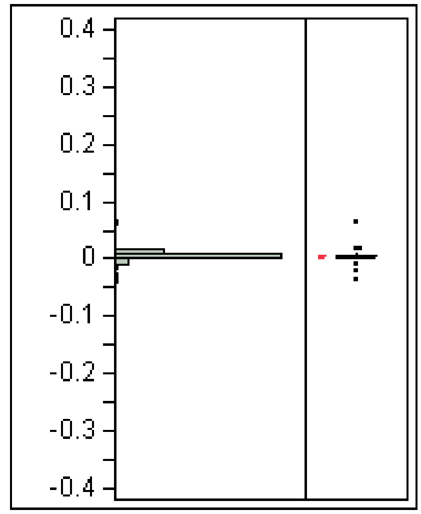
Quantiles

100.0%	maximum	0
99.5%		0
97.5%		0
90.0%		0
75.0%	quartile	0
50.0%	median	0
25.0%	quartile	0
10.0%		0
2.5%		0
0.5%		0
0.0%	minimum	0

Moments

Mean	0
Std Dev	0
Std Err Mean	0
Upper 95% Mean	0
Lower 95% Mean	0
N	115

%/C Y Axis Sense 85C



Quantiles

100.0%	maximum	0.0591
99.5%		0.0591
97.5%		0.0145
90.0%		0.0108
75.0%	quartile	0.0076
50.0%	median	0.0057
25.0%	quartile	0.0031
10.0%		0.00043
2.5%		-0.0142
0.5%		-0.0397
0.0%	minimum	-0.0397

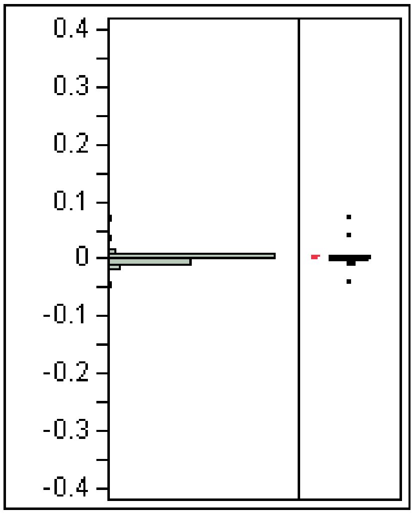
Moments

Mean	0.0053981
Std Dev	0.0082475
Std Err Mean	0.0007691
Upper 95% Mean	0.0069216
Lower 95% Mean	0.0038745
N	115

Figure 16. 2g/4g/8g Y-axis TCS (%/°C)

Distributions

%/C Z Axis Sense -40C



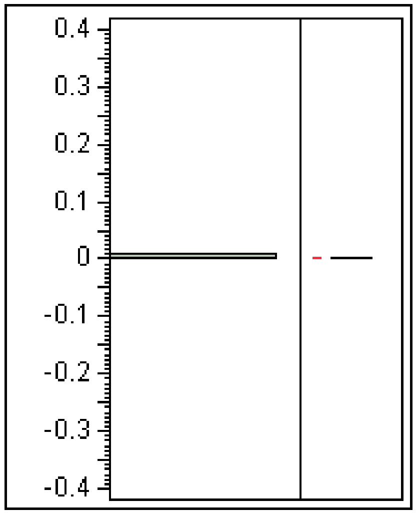
Quantiles

100.0%	maximum	0.0671
99.5%		0.0671
97.5%		0.0113
90.0%		0.0059
75.0%	quartile	0.0039
50.0%	median	0.0016
25.0%	quartile	-0.0014
10.0%		-0.0046
2.5%		-0.0137
0.5%		-0.0440
0.0%	minimum	-0.0440

Moments

Mean	0.0014675
Std Dev	0.0091351
Std Err Mean	0.0008482
Upper 95% Mean	0.0031476
Lower 95% Mean	-0.000213
N	116

%/C Z Axis Sense 25C



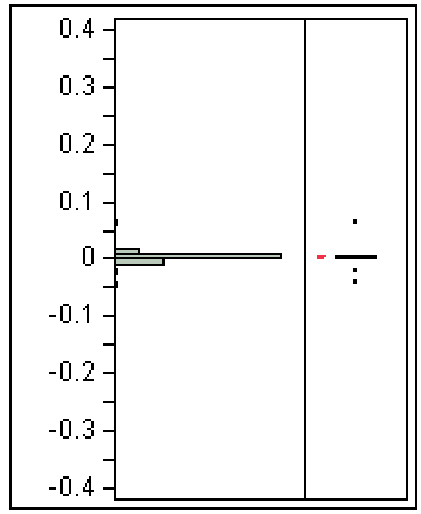
Quantiles

100.0%	maximum	0
99.5%		0
97.5%		0
90.0%		0
75.0%	quartile	0
50.0%	median	0
25.0%	quartile	0
10.0%		0
2.5%		0
0.5%		0
0.0%	minimum	0

Moments

Mean	0
Std Dev	0
Std Err Mean	0
Upper 95% Mean	0
Lower 95% Mean	0
N	116

%/C Z Axis Sense 85C



Quantiles

100.0%	maximum	0.0607
99.5%		0.0607
97.5%		0.0114
90.0%		0.0089
75.0%	quartile	0.0061
50.0%	median	0.0031
25.0%	quartile	0.00047
10.0%		-0.0017
2.5%		-0.0049
0.5%		-0.0446
0.0%	minimum	-0.0446

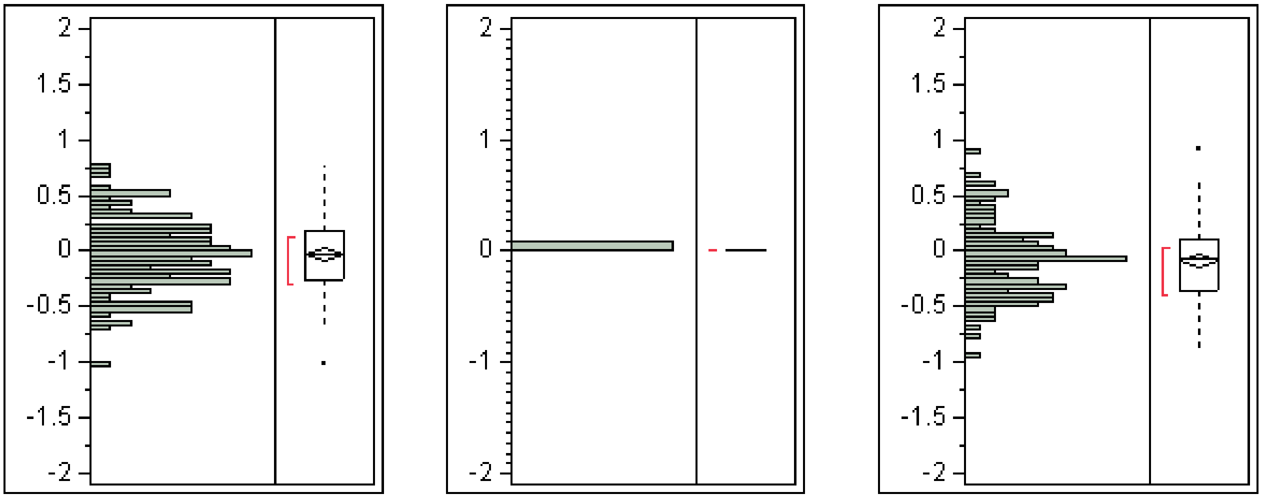
Moments

Mean	0.0032194
Std Dev	0.0082346
Std Err Mean	0.0007646
Upper 95% Mean	0.0047339
Lower 95% Mean	0.001705
N	116

Figure 17. 2g/4g/8g Z-axis TCS (%/°C)

Distributions

mg/C X Axis Offset -40C	mg/C X Axis Offset 25C	mg/C X Axis Offset 85C



Quantiles

	mg/C X Axis Offset -40C	mg/C X Axis Offset 25C	mg/C X Axis Offset 85C
100.0% maximum	0.779	0	0.8987
99.5%	0.779	0	0.8987
97.5%	0.691	0	0.6096
90.0%	0.402	0	0.3963
75.0% quartile	0.188	0	0.1144
50.0% median	-0.026	0	-0.0698
25.0% quartile	-0.254	0	-0.3569
10.0%	-0.496	0	-0.4921
2.5%	-0.664	0	-0.6805
0.5%	-1.041	0	-0.9411
0.0% minimum	-1.041	0	-0.9411

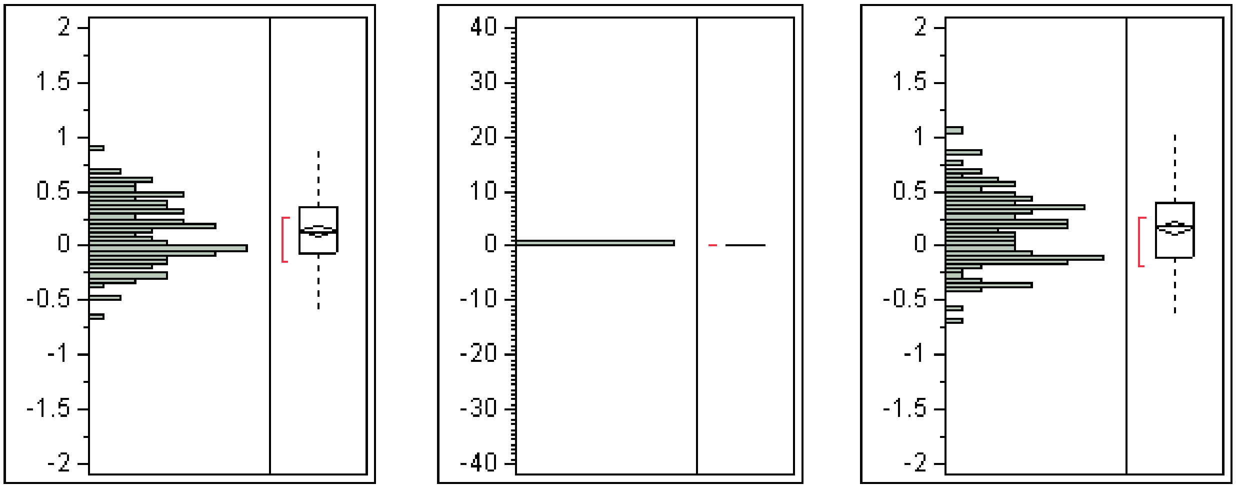
Moments

	mg/C X Axis Offset -40C	mg/C X Axis Offset 25C	mg/C X Axis Offset 85C
Mean	-0.032837	0	-0.086591
Std Dev	0.329128	0	0.3334645
Std Err Mean	0.0305588	0	0.0309614
Upper 95% Mean	0.0276945	0	-0.025263
Lower 95% Mean	-0.093368	0	-0.14792
N	116	116	116

Figure 18. 2g/4g/8g X-axis TCO (mg/°C)

Distributions

mg/C Y Axis Offset -40C	mg/C Y Axis Offset 25C	mg/C Y Axis Offset 85C



Quantiles

		mg/C Y Axis Offset -40C	mg/C Y Axis Offset 25C	mg/C Y Axis Offset 85C
100.0%	maximum	0.8778	0	1.048
99.5%		0.8778	0	1.048
97.5%		0.7008	0	0.846
90.0%		0.5321	0	0.560
75.0%	quartile	0.3565	0	0.387
50.0%	median	0.1341	0	0.185
25.0%	quartile	-0.0607	0	-0.098
10.0%		-0.2693	0	-0.276
2.5%		-0.4711	0	-0.406
0.5%		-0.6254	0	-0.686
0.0%	minimum	-0.6254	0	-0.686

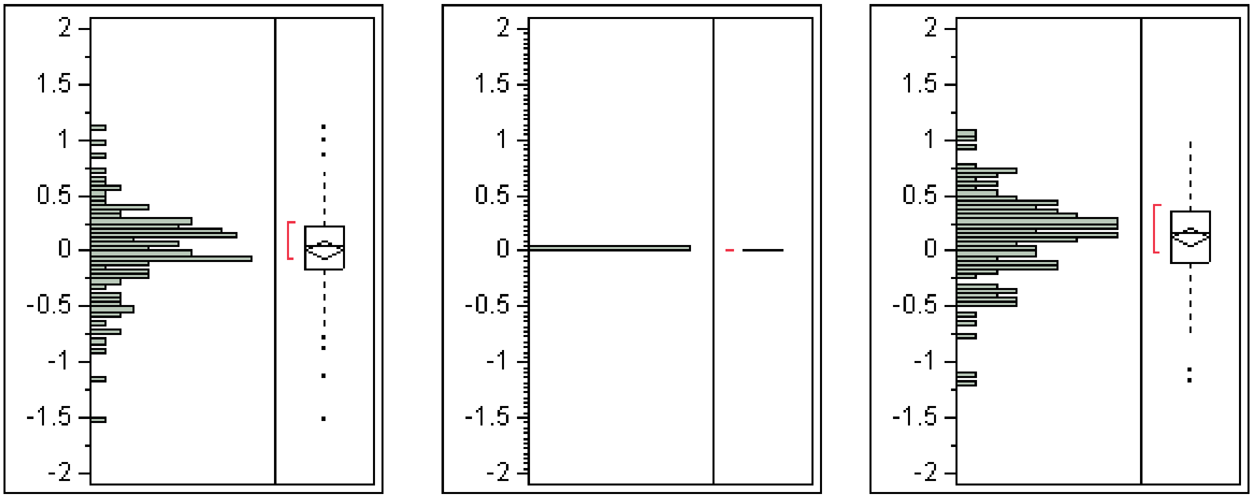
Moments

	mg/C Y Axis Offset -40C	mg/C Y Axis Offset 25C	mg/C Y Axis Offset 85C
Mean	0.1367918	0	0.1605936
Std Dev	0.2915227	0	0.3231423
Std Err Mean	0.0271846	0	0.0301332
Upper 95% Mean	0.1906444	0	0.2202872
Lower 95% Mean	0.0829393	0	0.1009
N	115	115	115

Figure 19. 2g/4g/8g Y-axis TCO (mg/°C)

Distributions

	mg/C Z Axis Offset -40C	mg/C Z Axis Offset 25C	mg/C Z Axis Offset 85C



Quantiles

		mg/C Z Axis Offset -40C	mg/C Z Axis Offset 25C	mg/C Z Axis Offset 85C
100.0%	maximum	1.087	0	1.055
99.5%		1.087	0	1.055
97.5%		0.846	0	0.936
90.0%		0.420	0	0.605
75.0%	quartile	0.225	0	0.366
50.0%	median	0.046	0	0.167
25.0%	quartile	-0.168	0	-0.099
10.0%		-0.508	0	-0.423
2.5%		-0.918	0	-0.791
0.5%		-1.531	0	-1.197
0.0%	minimum	-1.531	0	-1.197

Moments

	mg/C Z Axis Offset -40C	mg/C Z Axis Offset 25C	mg/C Z Axis Offset 85C
Mean	0.0139184	0	0.128959
Std Dev	0.3946105	0	0.390181
Std Err Mean	0.0366387	0	0.0362274
Upper 95% Mean	0.0864926	0	0.2007185
Lower 95% Mean	-0.058656	0	0.0571995
N	116	116	116

Figure 20. 2g/4g/8g Z-axis TCO (mg/°C)

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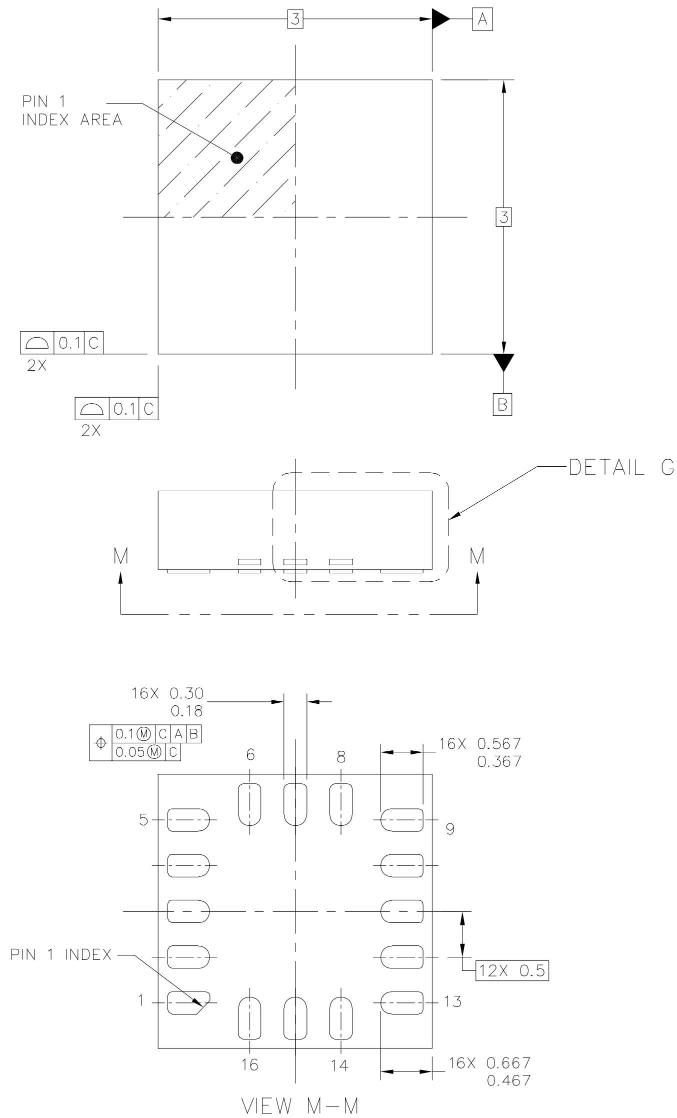

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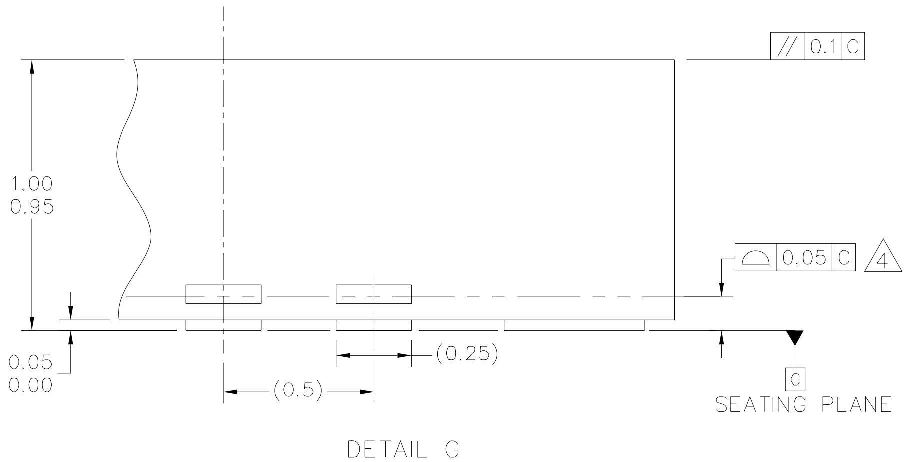

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