19-0813; Rev 2; 12/10

EVALUATION KIT AVAILABLE

DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

MAX3814

General Description

The MAX3814 TMDS™ EQ/driver IC compensates for FR-4 and cable losses up to the DVI™/HDMI® transmit connector and provides a fully compliant DVI/HDMI TMDS output. The device can also be used in DVI/HDMI cable applications to extend reach and improve jitter margin of cable channels at the receive-side connector.

The on-chip TMDS drivers operate at a standard current level for implementing a typical DVI/HDMI non-back-terminated transmitter, as well as a 50% higher current mode for using a 200Ω back termination resistor (nonmatching) to achieve a 10dB return loss. Typical DVI/HDMI output drivers contribute to reflection problems between the connector and a typical high-impedance (open) DVI/HDMI Tx output. The selectable output current (LEVEL pin) gives the option of partial back termination (e.g., differentially connected 200Ω) to mitigate the reflection problem effectively while keeping common-mode offset to a minimum.

The 4-channel implementation treats all channels identically. To allow board layout flexibility for DVI and HDMI connectors, which have different channel order, the clock and data channels can be arbitrarily assigned.

The MAX3814 operates from a 3.3V power supply, standard for DVI/HDMI applications, and is packaged in a 5mm x 5mm x 0.1mm, 32-pin TQFP package.

Applications

Laptop PC TMDS Equalizer and Driver

Docking Station TMDS Equalizer and Driver

Cable TMDS Equalizer

Features

- **Equalizes FR-4 Board Microstrip and Cable HF Losses Up to 15dB at 825MHz for Operation at 0.25Gbps to 1.65Gbps**
- **Compatible with HDMI 1.3**
- **Less Than 0.2UI$_{P-P}$ Residual Jitter at 1.65Gbps for 0 to 15dB Channel Loss at 825MHz**
- **Input Terminations: 50Ω (Each Side to V_{CC}) ±10%**
- **Output of Driver is a Fully DVI/HDMI TMDS-Compatible Cable Driver**
- **Output Amplitude: 1.05V$_{P-P}$ Differential**
- **Enable Pin to Select Normal Operation or Power-Down Mode**
- **LEVEL Pin to Select Output Current for Use With or Without Back Termination**
- **32-Pin TQFP for Four Channels; Any Channel Can Be Either a TMDS Data or Clock Signal**
- **V_{CC} = 3.3V; Signal Pins Have Absolute Max Ratings of 5.5V (for Fault Conditions)**

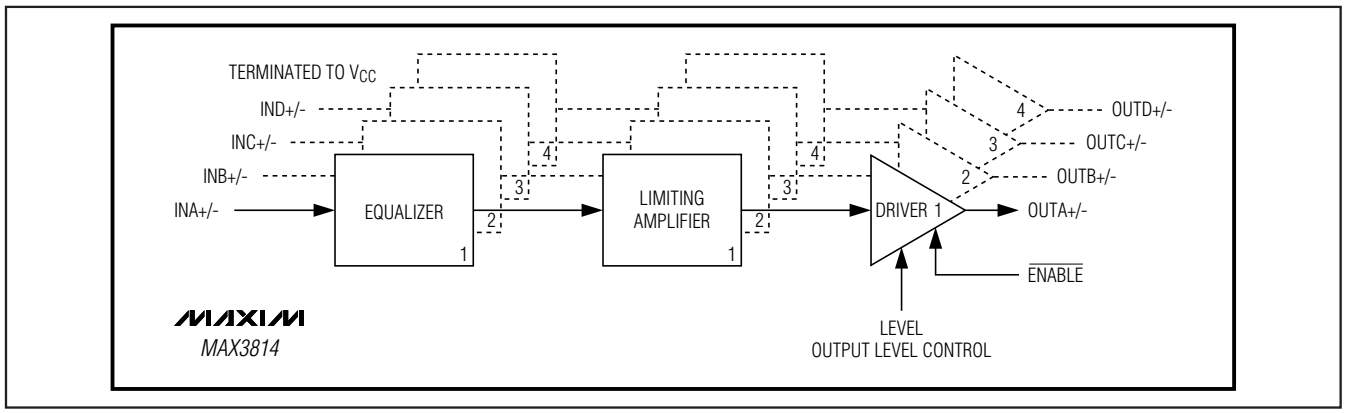
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3814CHJ+	0°C to +70°C	32 TQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration appears at end of data sheet.

Simplified Functional Diagram



TMDS is a trademark of Silicon Image, Inc.
DVI is a trademark of Digital Display Working Group.
HDMI is a registered trademark and registered service mark of HDMI Licensing, LCC.

DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

ABSOLUTE MAXIMUM RATINGS

Termination-Supply Voltage Range.....-0.5V to +4.0V
Signal Voltage Range on Any One Signal Wire ....-0.5V to +4.0V
CML Common-Mode Voltage Range on
Any I/O Pair (sustained) .....-0.5V to +5.5V
CML Common-Mode Voltage Range on Any I/O Pair
(sustained, within V_{CC} and GND) ...-3.3V to +3.3V, Differential
CML Output Loading (termination).....0Ω to Open
Operating Ambient Temperature Range .....0°C to +70°C
Storage Ambient Temperature Range.....-40°C to +150°C
ESD Human Body Model, Any Pin 2000V
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATION TABLES

(Typical values measured at V_{CC} = 3.3V, T_A = +25°C; external terminations = 50Ω ±1%; min/max values valid over V_{CC} = 3.3V ±0.3V, T_A = 0°C to +70°C; with external terminations = 50Ω ±1% to voltage = 3.3V ±0.7V. Tested at 1.65Gbps. AC parameters guaranteed by design and characterization.)

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Operating Ambient Temperature			0	25	70	°C
Data Rate			0.25		1.65	Gbps
Maximum Channel Loss		At 825MHz, FR-4 microstrip compensate on curve	15			dB
Source Output Rise/Fall Time		20% to 80%, measured at source transmitter (input to channel)			240	ps
Differential Input-Voltage Swing		Measured at source transmitter (input to channel)	700	1050	1400	mV_{P-P}
Maximum Supply Noise Tolerance		DC-5000kHz, all specifications maintained		50		mV_{P-P}

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC PARAMETERS					
Supply Current			110	140	mA

TMDS EQUALIZER PERFORMANCE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Residual Output Jitter (15 x RJ_{RMS} + DJ) from 0.25Gbps to 1.65Gbps	Subtract source jitter for DJ, 0 to 15dB FR4 loss at 825MHz (Note 1)			0.2	UI_{P-P}

SPECIFICATION TABLES (continued)

(Typical values measured at V_{CC} = 3.3V, T_A = +25°C; external terminations = 50Ω ±1%; min/max values valid over V_{CC} = 3.3V ±0.3V, T_A = 0°C to +70°C; with external terminations = 50Ω ±1% to voltage = 3.3V ±0.7V. Tested at 1.65Gbps. AC parameters guaranteed by design and characterization.)

CML INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC PARAMETERS					
Common-Mode Input Voltage		V_{CC} - 400		V_{CC} + 100	mV
Input Termination Voltage	When disconnected from source	V_{CC} - 10		V_{CC} + 10	mV
Single-Ended Input Termination	With 50Ω load, each side to V_{CC}	45	50	55	Ω
AC PARAMETERS					
Differential Input Return Loss	< 1.6GHz		14		dB

CML OUTPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC PARAMETERS					
Differential Output-Voltage Swing	With 50Ω load, each side to V_{CC}; LEVEL = low	900	1050	1200	mV_{P-P}
	With 50Ω load, each side to V_{CC}; LEVEL = high; 200Ω back termination	900	1050	1200	
Single-Ended High Output Voltage	LEVEL = low	V_{CC} - 10		V_{CC} + 10	mV
Single-Ended Low Output Voltage	LEVEL = low	V_{CC} - 600		V_{CC} - 400	mV
Output Voltage When $\overline{ENABLE}$ Disabled	LEVEL = low, $\overline{ENABLE}$ = high	V_{CC} - 10		V_{CC} + 10	mV
AC PARAMETERS					
Output, Rise/Fall Time	20% to 80%; with 50Ω load, each side to V_{CC}	80	170	230	ps

DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

SPECIFICATION TABLES (continued)

(Typical values measured at V_{CC} = 3.3V, T_A = +25°C; external terminations = 50Ω ±1%; min/max values valid over V_{CC} = 3.3V ±0.3V, T_A = 0°C to +70°C; with external terminations = 50Ω ±1% to voltage = 3.3V ±0.7V. Tested at 1.65Gbps. AC parameters guaranteed by design and characterization.)

LVTTL/LVCMOS AND OPEN-COLLECTOR LVTTL

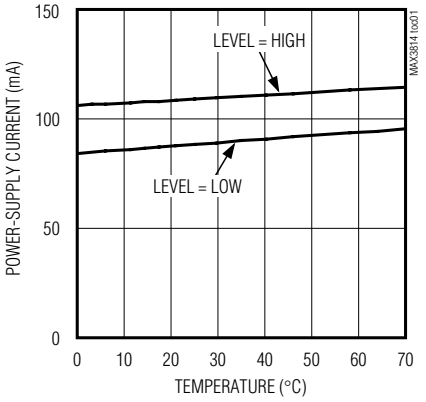
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC PARAMETERS					
LVTTL Input High Voltage		2.0			V
LVTTL Input Low Voltage				0.8	V
LVTTL Input High Current		-100		+100	µA
LVTTL Input Low Current		-100		+100	µA

Note 1: The specified FR-4 loss is from 12-mil traces, 7-mil spacing, and 6-mil depth (Prepreg) with no solder mask. The test pattern is a 2^7 - 1, 20 zeros, inverted 2^7 - 1, and 20 ones.

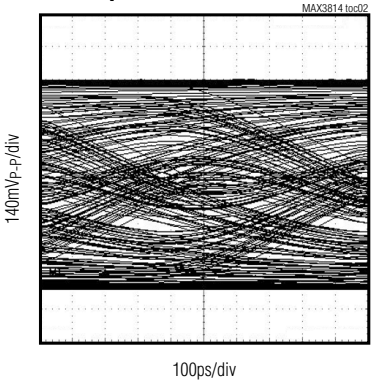
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Residual jitter is measured directly from the eye diagram histogram after 5000 hits.)

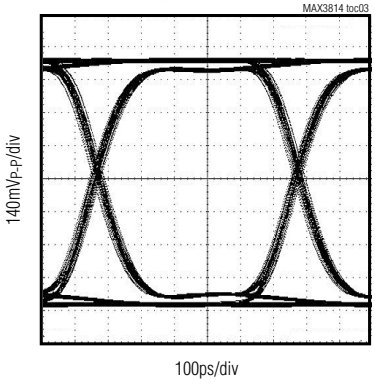
POWER-SUPPLY CURRENT vs. TEMPERATURE



MAX3814 INPUT: EYE DIAGRAM OF 1.65Gbps DATA AFTER 80in OF FR-4



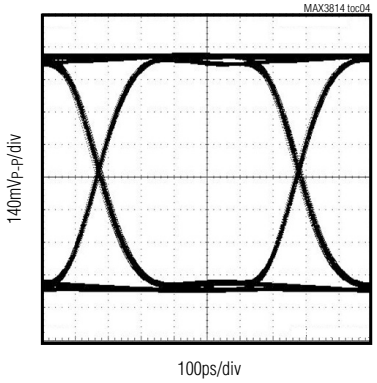
MAX3814 OUTPUT: EYE DIAGRAM OF MAX3814 EQUALIZING 1.65Gbps DATA AFTER 80in OF FR-4



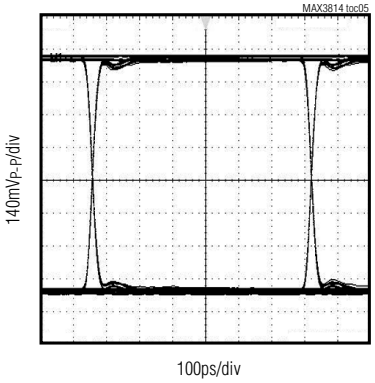
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Residual jitter is measured directly from the eye diagram histogram after 5000 hits.)

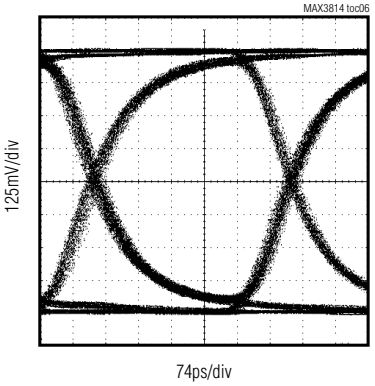
MAX3814 OUTPUT: 1.65Gbps DATA AFTER 30ft OF TENSOLITE 28 AWG CABLE



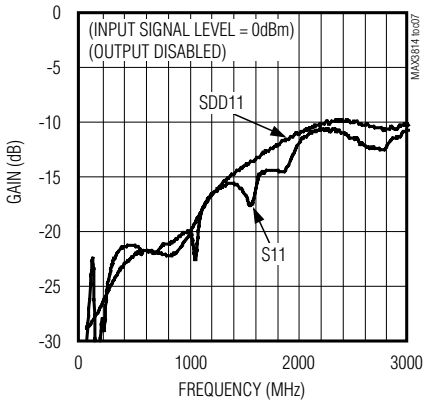
MAX3814 OUTPUT: 250Mbps DATA AFTER 30ft OF TENSOLITE 28 AWG CABLE



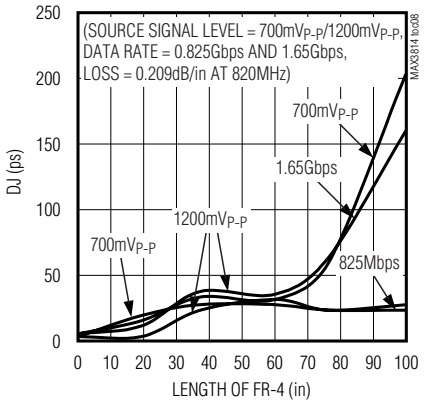
MAX3814 OUTPUT: 2.25Gbps DATA AFTER 33ft OF 24 AWG SPECTRA STRIP CABLE



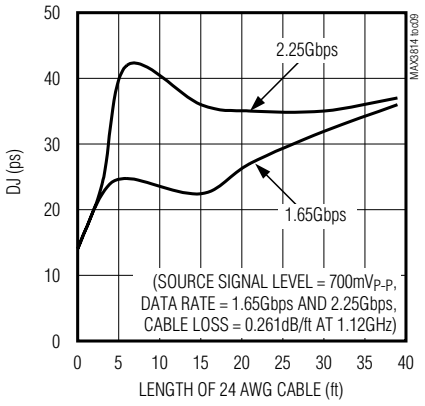
SINGLE-ENDED/DIFFERENTIAL INPUT RETURN LOSS (S11/SDD11)



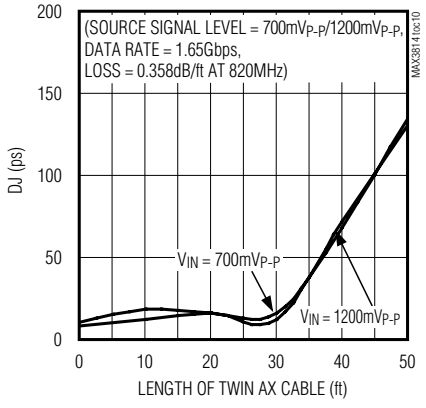
DETERMINISTIC JITTER vs. LENGTH OF FR-4 BOARD



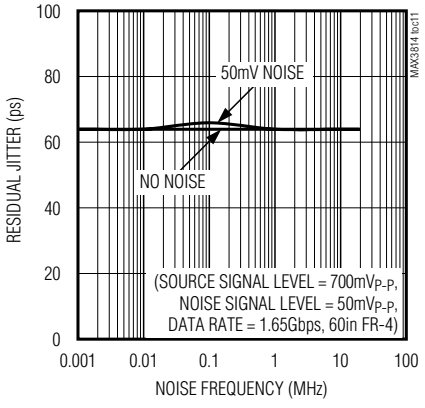
DETERMINISTIC JITTER vs. LENGTH OF 24 AWG CABLE



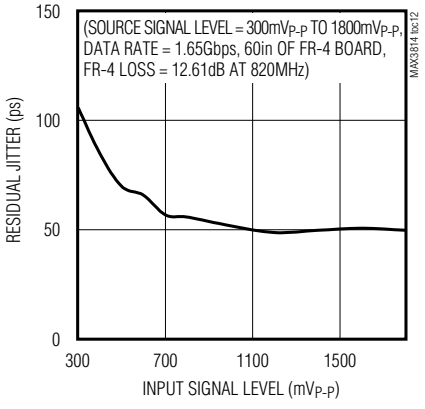
DETERMINISTIC JITTER FOR 28 AWG TWIN AX CABLE



RESIDUAL JITTER DUE TO POWER-SUPPLY SINUSOIDAL NOISE



RESIDUAL JITTER



DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

Pin Description

PIN	NAME	FUNCTION
1, 8, 17, 24	N.C.	No Connection. Not internally connected.
2	INB+	Positive TMDS Input, CML
3	INB-	Negative TMDS Input, CML
4, 5, 9, 32	V_{CC}	Power Supply. All pins must be connected to V_{CC}.
6	INC+	Positive TMDS Input, CML
7	INC-	Negative TMDS Input, CML
10	IND+	Positive TMDS Input, CML
11	IND-	Negative TMDS Input, CML
12	$\overline{ENABLE}$	Active-Low Enable Input, LVTTL. High to disable, outputs off. Low to enable, outputs on.
13, 16, 20, 21, 25, 28	V_{EE}	Negative Power Supply (Ground)
14	OUTD-	Negative TMDS Output, CML
15	OUTD+	Positive TMDS Output, CML
18	OUTC-	Negative TMDS Output, CML
19	OUTC+	Positive TMDS Output, CML
22	OUTB-	Negative TMDS Output, CML
23	OUTB+	Positive TMDS Output, CML
26	OUTA-	Negative TMDS Output, CML
27	OUTA+	Positive TMDS Output, CML
29	LEVEL	Output Current Level Control, LVTTL. Low for 10mA output currents. High for 15mA currents. Used for 200Ω back differential termination resistors.
30	INA+	Positive TMDS Input, CML
31	INA-	Negative TMDS Input, CML

Detailed Description

The MAX3814 TMDS equalizer/driver accepts differential CML input data rates from 250Mbps to 1.65Gbps. It consists of four differential CML input buffers, four independent fixed equalizers, four limiting amplifiers, and four differential CML output buffers (Figure 1). The MAX3814 functions both as an equalizer and as a driver.

As an equalizer the MAX3814 automatically adjusts for attenuation levels up to 16dB at 825MHz from either dielectric board losses or skin-effect losses in copper cable.

As a driver the MAX3814 provides CML outputs. The CML output is normally open (i.e., no back termination) and is DC-coupled by transmission line to a termination at the far end per DVI/HDMI standards. The MAX3814 provides nominally 10mA output-switching currents. However, with the MAX3814, there is a selectable higher current drive to accommodate a differential 200Ω back termination resistor while maintaining the differential swing of 1000mV$_{P-P}$. This 200Ω back termination resistor serves to dampen signal reflections returning to the device from discontinuities in the channel such as DVI or HDMI connectors, providing a 10dB return loss. See the *CML Inputs and Outputs* section for more information.

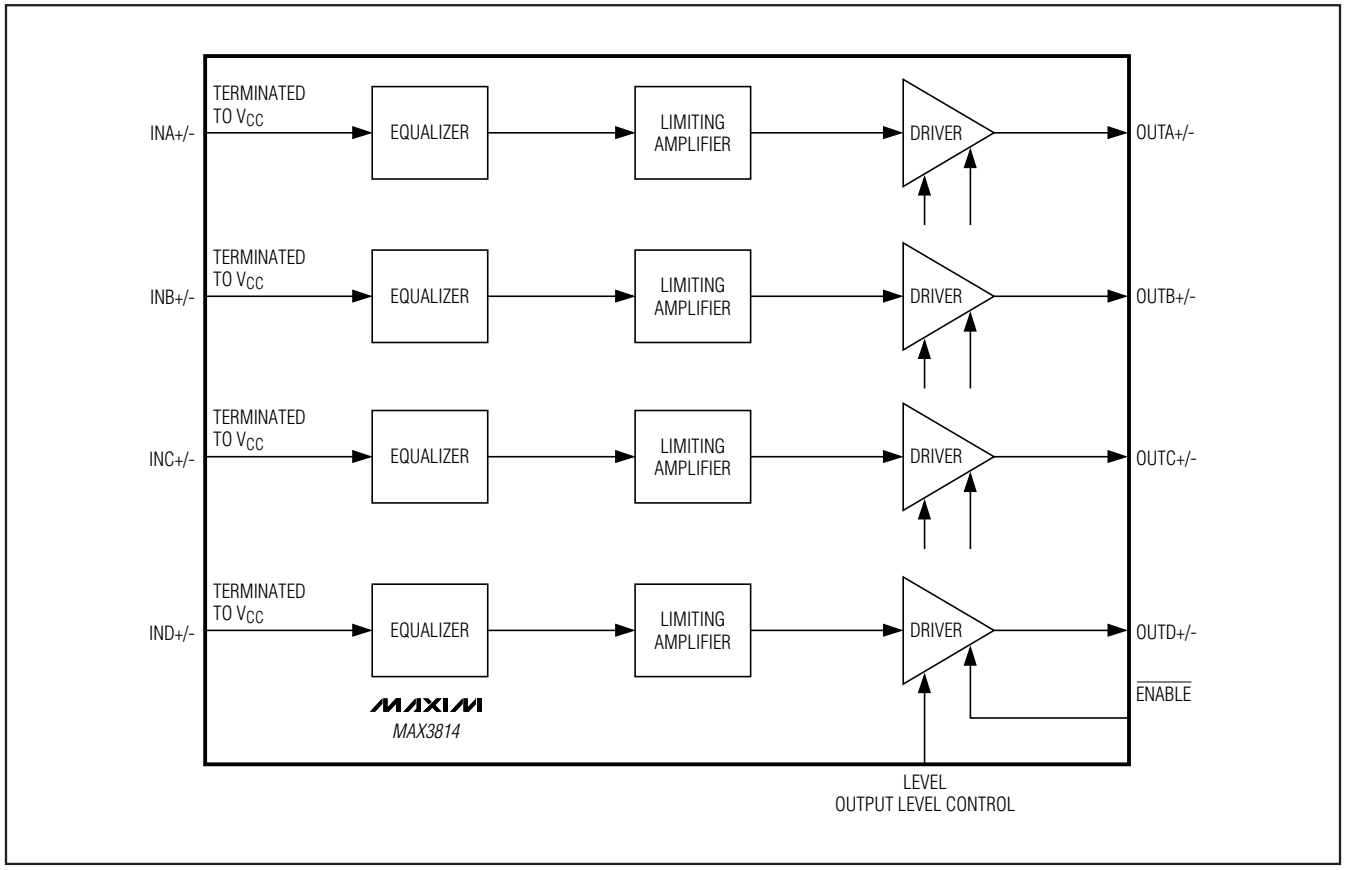


Figure 1. Functional Diagram

DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

CML Inputs and Outputs

The input buffers and the output drivers are current-mode logic (CML). See Figures 2, 3, and 4.

The input buffers consist of a 50Ω load resistor connected to V_{CC} and the input connected to a differential equalizer.

The output drivers are open-collector. The current in these outputs can be adjusted to 10mA or 15mA with the control pin LEVEL. For 10mA operation, each open-collector output drives through a transmission line to a 50Ω pullup of the next stage, as shown in Figure 3. For recommended 15mA operation, the two outputs are bridged by an external 200Ω back termination resistor that is subsequently pulled up by a 50Ω resistor of the next stage, as shown in Figure 4. The ESD structure permits signals to achieve 5.5V absolute maximum ratings, high common-mode range, and compatibility to HDMI testing. The back termination resistor should be placed as close as possible to the MAX3814 in the layout.

The ESD protection for both the input and output circuitry consists of diodes connected to a transient voltage suppressor clamp shown as a Schottky diode in Figures 2, 3, and 4. For more information about the function of the suppressor clamp, refer to the *Detailed Description* section of the MAX3208E data sheet (**www.maxim-ic.com/MAX3208E**).

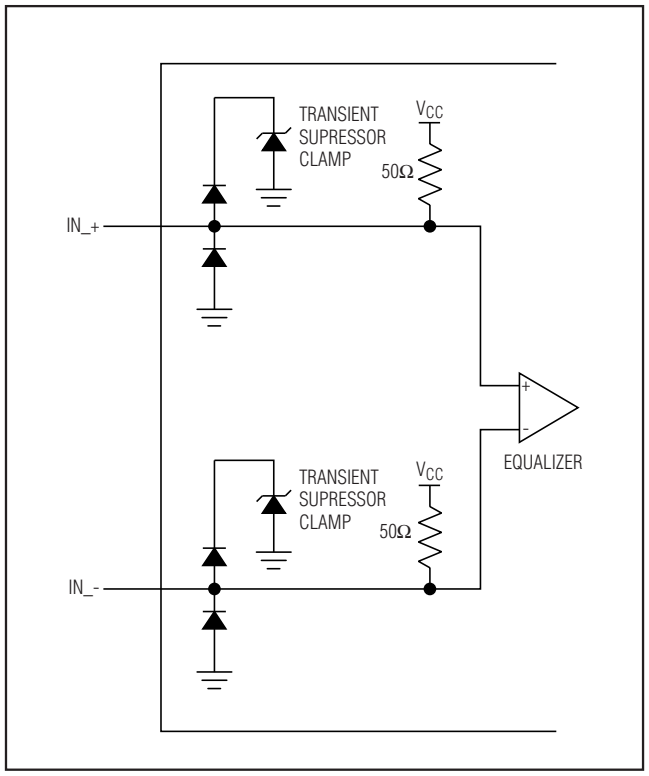


Figure 2. Simplified Input Circuit

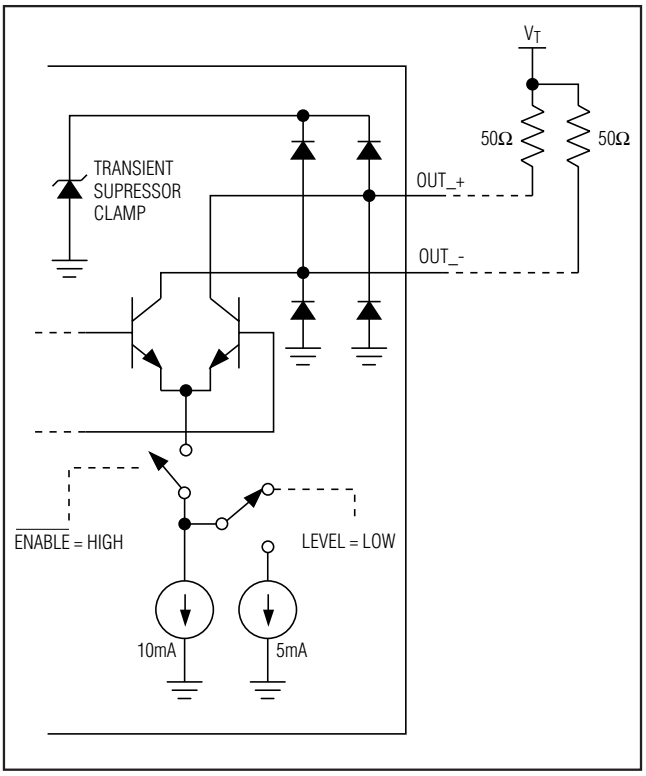


Figure 3. Simplified Output Circuit Without Back Termination Resistor

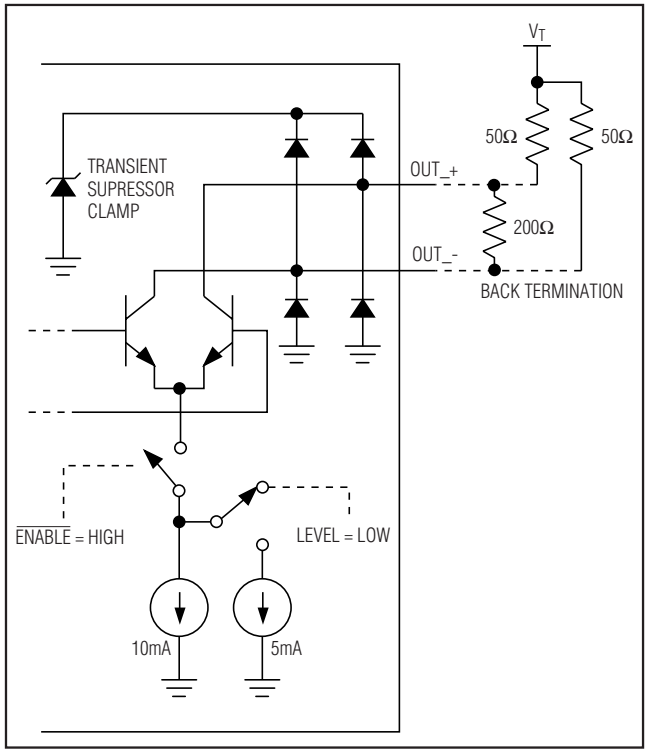


Figure 4. Simplified Output Circuit with Back Termination Resistor

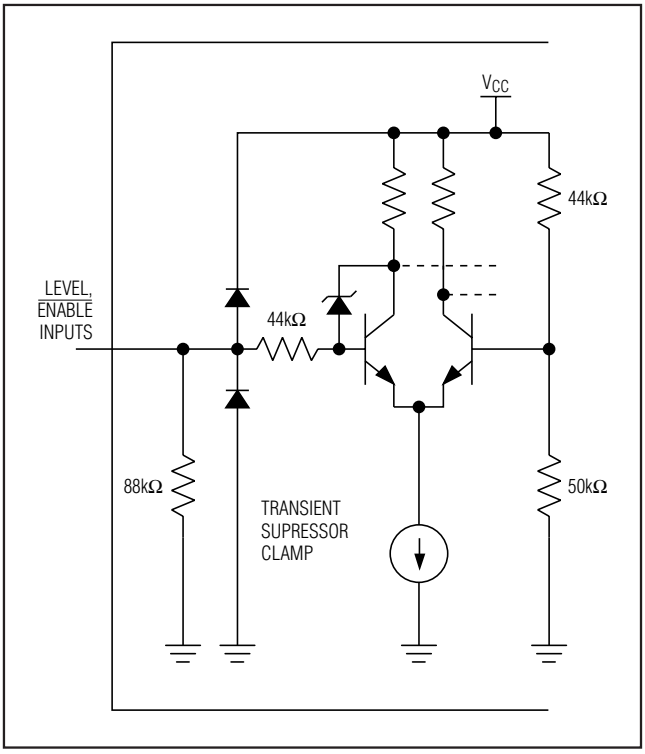


Figure 5. Simplified Input Circuitry for Output Level (LEVEL) and Enable (ENABLE) Control

Output Enable Control

The ENABLE pin is an LVTTL input that allows the user to shut off the output-collector currents, thereby reducing power consumption of the device. Forcing this pin high turns the output currents off; forcing this pin low (normal operation) turns the currents on.

Figure 5 shows a simplified circuit for both the output and enable controls.

Applications Information

Figure 6a shows a typical TMDS channel from a graphics board of a laptop computer to a remote display. Maintaining a 100Ω differential impedance for this channel has its challenges. Besides proper board layout of traces, there are multiple reflection points (A to H). For example, at interface F in Figure 6a, a circular arrow shows a reflection at the connector of a remote display. When these reflections hit another interface, they reflect again and thus become echoes corrupting the incident signal. In Figure 6b, the MAX3814 is used to equalize losses, isolate reflections, and redrive the transmission line with high fidelity.

DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

Laptop PC TMDS Equalizer and Driver

As shown at location XX in Figure 6b, the MAX3814 equalizes trace losses and redrives the TMDS outputs at the docking connector. The 200Ω resistor at the output of the MAX3814 absorbs reflections from the docking connector.

Dock or Port Expander

The MAX3814 can also be used on the dock or port expander as it equalizes loss, isolates the connector, and redrives TMDS output signals at location YY as shown in Figure 6b. Similarly, with the previous application, the 200Ω resistor at the output of the MAX3814 absorbs reflections in this case from the DVI or the HDMI connector.

An optional 2dB to 6dB attenuator pad can be used to absorb reflections between internal interface connections. If used, the attenuator pad must be a matched Pi or T attenuator network. The resulting flat through loss can be made by the excellent input sensitivity of the MAX3814 as shown in the *Typical Application Circuits*. The MAX3814's excellent input sensitivity allows the attenuated signal to be restored.

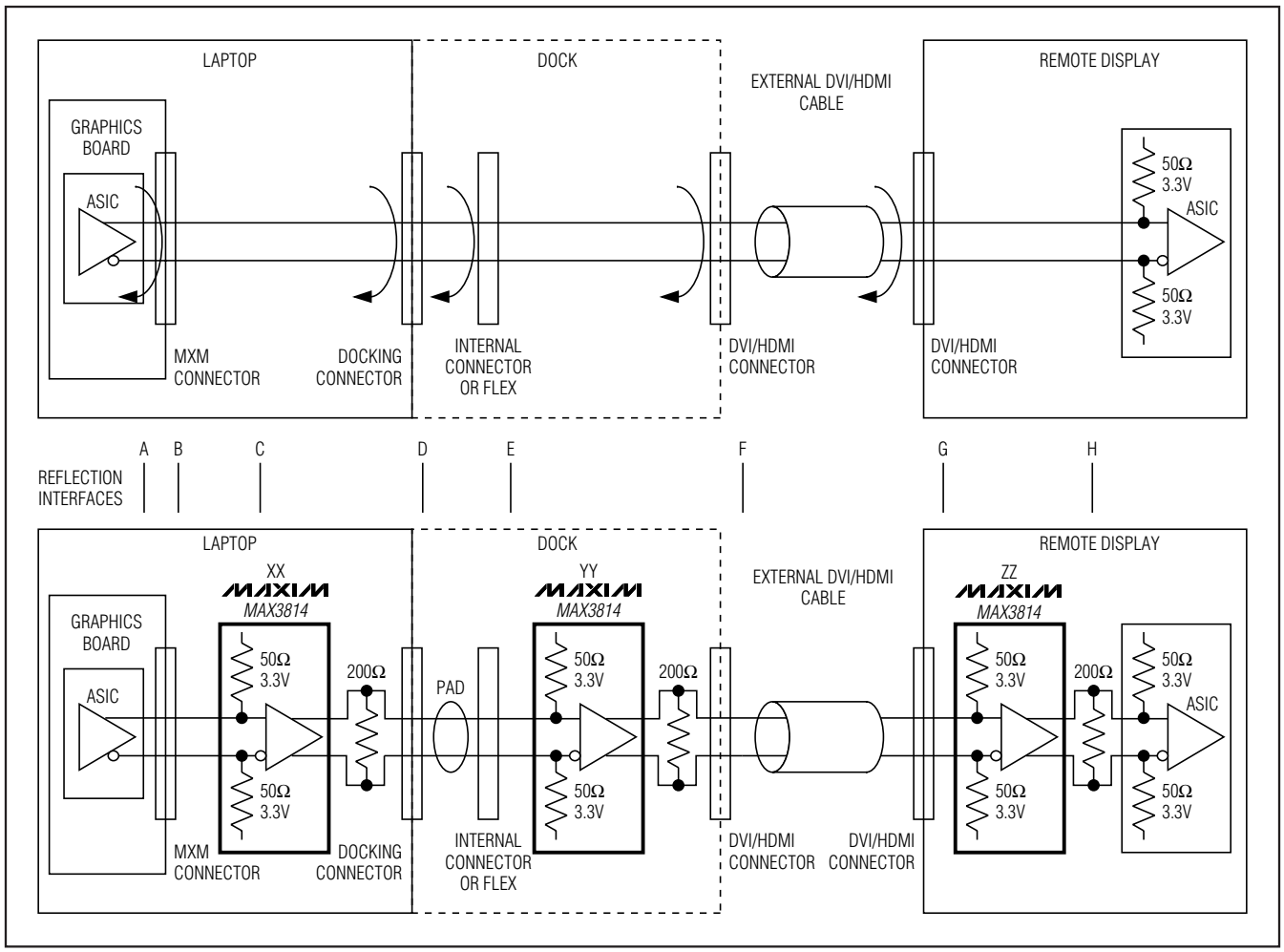


Figure 6a (top). Schematic Showing the TMDS Signal Channel from the Laptop Graphics Boards to the Remote Display. Possible Reflection Interfaces are Labeled A to H.

Figure 6b (bottom). Schematic Showing the Same Channel, with possible location of the MAX3814 to Equalize Losses, to Absorb Reflections, and to Redrive the Transmission Line.

Cable TMDS Equalizer

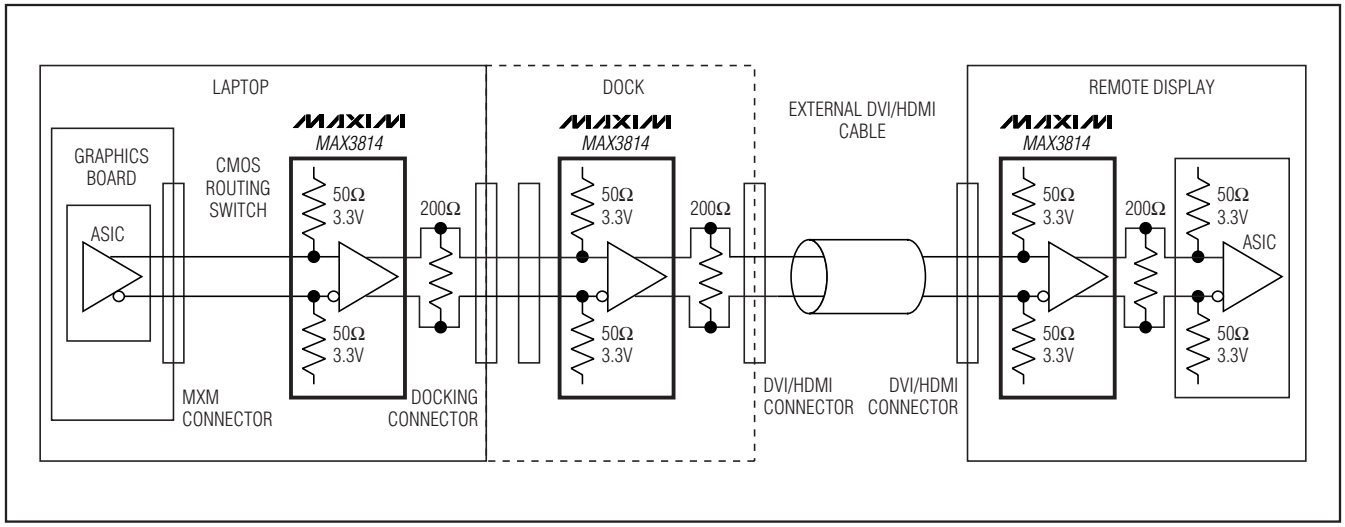
The MAX3814 is useful in providing equalization for cables losses at location ZZ, at the input DVI/HDMI connector of the remote display. It can equalize cable lengths of 15 meters of 26 AWG wire and 12 meters of 28 AWG wire. Again, the 200Ω resistor placed at the output of the MAX3814 absorbs reflections from the imperfect termination of the ASIC or imperfect transmission-line interconnect.

Layout Considerations

The TMDS CML inputs are the most critical paths for the MAX3814 and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3814.

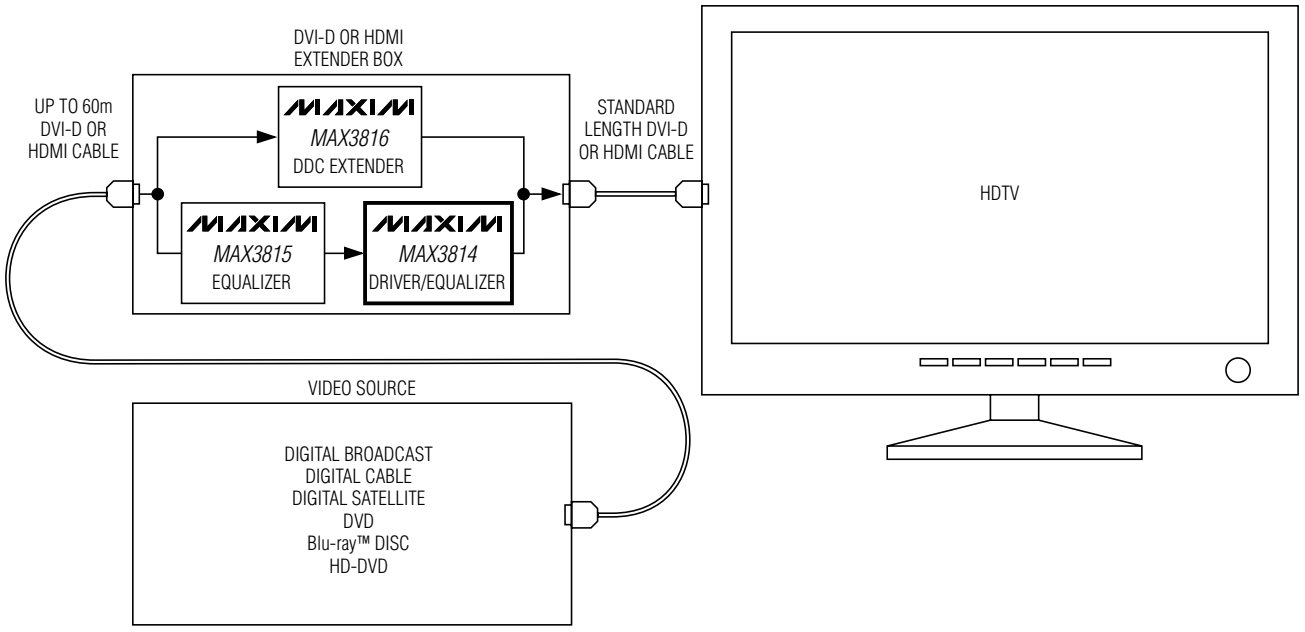
- The data and clock inputs should be wired directly between the cable connector and IC without stubs.
- The 4-channel implementation treats all channels identically. Input and output data channel designations are only a guide. Polarity assignments can be swapped and channel paths can be interchanged.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground-path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the DVI and HDMI inputs.
- Maintain a 100Ω differential transmission line impedance into and out of the MAX3814.
- To minimize possible reflections, choose the 200Ω back termination option. Place this resistor as close to the MAX3814 as possible.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Refer to the schematic and board layers of the MAX3814EVKIT.

Typical Application Circuits

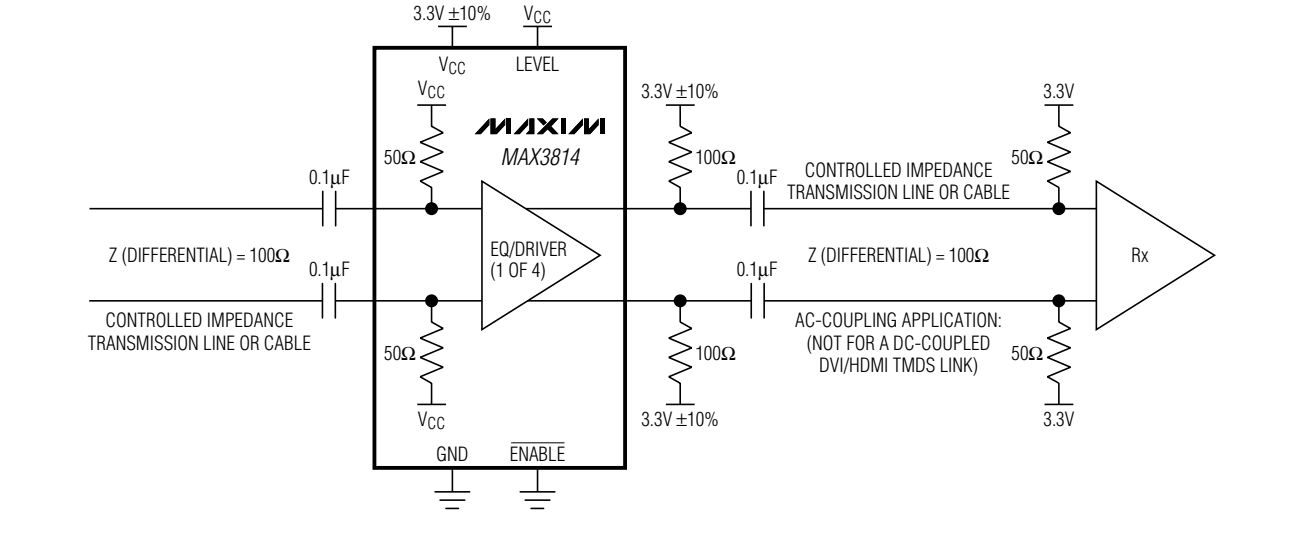


DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

Typical Application Circuits (continued)

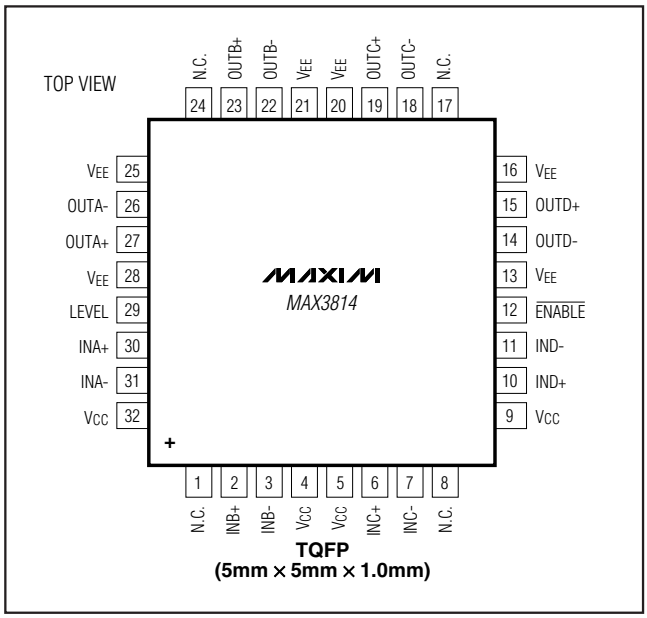


Blu-ray is a trademark of Blu-ray Disc Association.



DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

Pin Configuration



TQFP
(5mm × 5mm × 1.0mm)

Chip Information

PROCESS: SiGe BiPOLAR

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFP	H32+1	21-0110	90-0149

DVI/HDMI TMDS FR-4 and Cable Equalizer/Driver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/07	Initial release	—
1	9/07	Corrected T_A = 0°C to +85°C to T_A = 0°C to +70°C in the *Specification Tables* globals; replaced the package outline drawing with the *Package Information* table	2, 3, 4, 13
2	12/10	Changed the operating ambient temperature max from 85°C (max) to 70°C (max) in the *Operating Conditions* table; added the package code and land pattern no. to the *Package Information* table	2, 13