

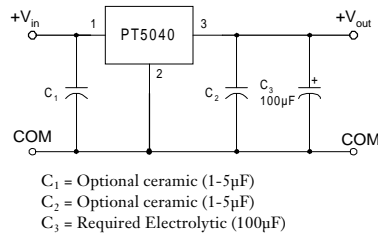
Features

- Wide Input Voltage Range
- 85% Efficiency
- Internal Over-Temperature Protection
- Laser-trimmed Output Voltage
- Soft Start
- 5-Pin Mount Option (Suffixes L & M)

Description

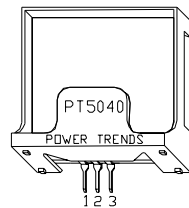
The PT5040 is a series of 3-pin boost-voltage Integrated Switching Regulators (ISRs). These ISRs are designed for use with +5V bus systems that require an additional regulated +8V to +20V with up to 1A of output current. These ISRs are packaged in the 3-pin, single in-line pin (SIP) package configuration.

Standard Application



Pin-Out Information

Pin	Function
1	V_{in}
2	GND
3	V_{out}



Ordering Information

- PT5041□ = +12 Volts
- PT5042□ = +15 Volts
- PT5044□ = +8 Volts
- PT5045□ = +9 Volts
- PT5046□ = +10 Volts
- PT5047□ = +18 Volts
- PT5048□ = +12.6 Volts
- PT5049□ = +20 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code*
Vertical	N	(EAD)
Horizontal	A	(EAA)
SMD	C	(EAC)
Horizontal, 2-pin Tab	M	(EAM)
SMD, 2-Pin Tab	L	(EAL)

* Previously known as package styles 100/110.
 (Reference the applicable package code drawing for the dimensions and PC board layout)

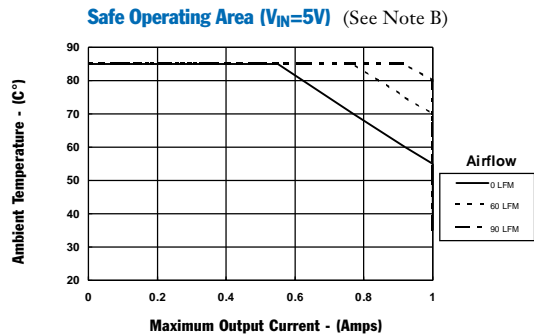
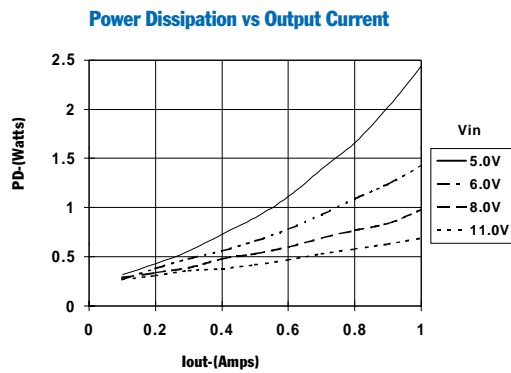
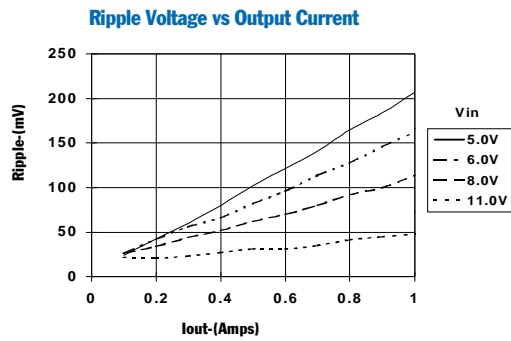
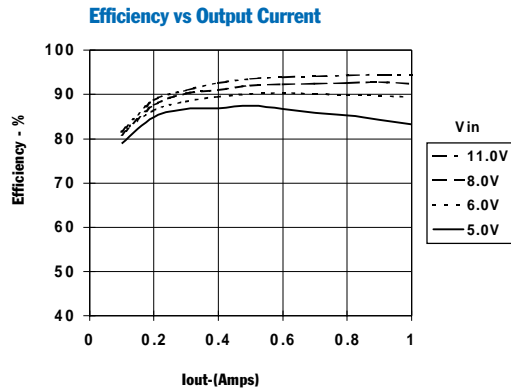
NOTE: Boost Topology ISRs are not Short-Circuit Protected.

Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 5\text{V}$, $I_o = I_{o,max}$, $C_3 = 100\mu\text{F}$)

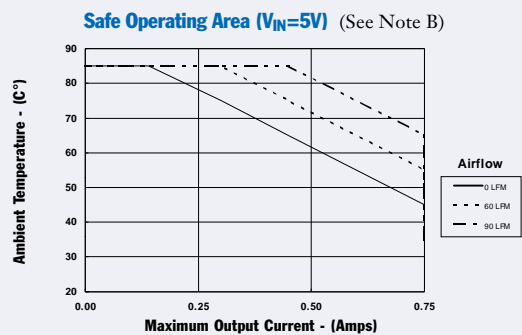
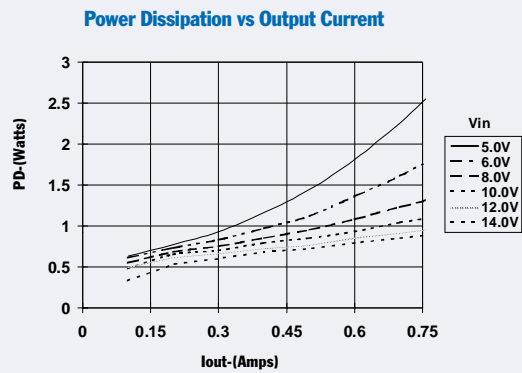
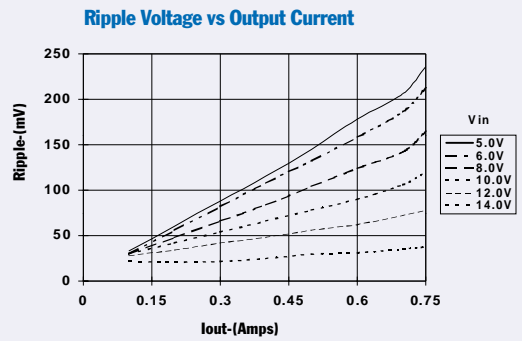
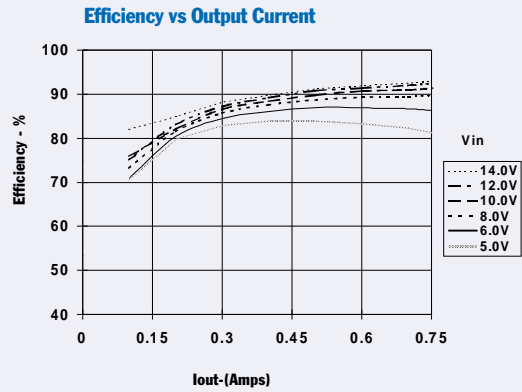
Characteristics	Symbol	Conditions	PT5040 SERIES			Units	
			Min	Typ	Max		
Output Current	I_o	Over V_{in} range	PT5049	0.1 (1)	—	0.5	A
			PT5047	0.1 (1)	—	0.6	
			PT5041/48	0.1 (1)	—	1.0	
			PT5042	0.1 (1)	—	0.75	
			PT5044	0.1 (1)	—	1.5	
			PT5045/46	0.1 (1)	—	1.2	
Input Voltage Range	V_{in}	Over I_o range	PT5047/5049	4.75	—	$(V_o - 1)$ 14	V
Output Voltage Tolerance	ΔV_o	Over V_{in} Range $T_a = -20^\circ\text{C}$ to SOA derating limit (3)	—	± 1.5	± 3.0	$\%V_o$	
Line Regulation	Reg_{line}	Over V_{in} range	—	± 0.5	± 1.0	$\%V_o$	
Load Regulation	Reg_{load}	$I_{o,min} \leq I_o \leq I_{o,max}$	—	± 0.5	± 1.0	$\%V_o$	
Efficiency	η	$I_o = 0.5\text{A}$	—	85	—	%	
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	—	± 2	± 5	$\%V_o$	
Transient Response	t_{tr} V_{os}	25% load change V_o over/undershoot	—	500	—	μSec	
			—	3.0	5.0	$\%V_o$	
Current Limit	I_{lim}	—	—	150 (2)	—	$\%I_{o,max}$	
Inrush Current	I_{ir} t_{ir}	On start up	—	5.5 (3)	—	A	
			—	1	—	mSec	
Switching Frequency	f_s	Over V_{in} and I_o ranges	$V_o < 15\text{V}$	500	650	800	kHz
			$V_o \geq 15\text{V}$	650	800	950	
Operating Temperature Range	T_a	—	-20	—	+85 (4)	$^\circ\text{C}$	
Thermal Resistance	θ_{pa}	Free Air Convection (40-60LFM)	—	40	—	$^\circ\text{C}/\text{W}$	
Storage Temperature	T_s	—	-40	—	+125	$^\circ\text{C}$	
Mechanical Shock	—	Per Mil-STD-883D, Method 2002.3 1 msec, Half Sine, mounted to a fixture	—	500	—	G's	
Mechanical Vibration Per Mil-STD-883D, 20-2000 Hz	—	Suffixes N, A, & C Suffixes L & M	—	5	—	G's	
			—	20 (5)	—		
Weight	—	Suffixes N, A, & C Suffixes L & M	—	4.5	—	grams	
			—	6.5	—		

- Notes:**
- (1) The ISR will operate at no load with reduced specifications.
 - (2) Boost topology ISRs are not short circuit protected.
 - (3) The inrush current stated is above the normal input current for the associated output load.
 - (4) See Safe Operating Area curves or consult the factory for the appropriate derating
 - (5) The tab pins on the 5-pin mount package types (suffixes L & M) must be soldered. For more information see the applicable package outline drawing.

PT5041, +12.0 VDC (See Note A)



PT5042, +15.0 VDC (See Note A)



Note A: Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.
Note B: Thermal derating graphs are developed in free-air convection cooling, which corresponds to approximately 40–60LFM of airflow.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT5041J	OBSOLETE	SIP MODULE	EAJ	3		TBD	Call TI	Call TI			
PT5044L	OBSOLETE	SIP MODULE	EAL	3		TBD	Call TI	Call TI			
PT5045C	OBSOLETE	SIP MODULE	EAC	3		TBD	Call TI	Call TI			
PT5046A	OBSOLETE	SIP MODULE	EAA	3		TBD	Call TI	Call TI			
PT5048C	OBSOLETE	SIP MODULE	EAC	3		TBD	Call TI	Call TI			
PT5049C	OBSOLETE	SIP MODULE	EAC	3		TBD	Call TI	Call TI	-20 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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