MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

WITH ±15-kV ESD PROTECTION SLLS410I – JANUARY 2000 – REVISED JANUARY 2004

- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current . . . 300 μA Typical
- External Capacitors . . . 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s)
 SNx5C3232
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

description/ordering information

D, DB, D	D, DB, DW, OR PW PACKAGE (TOP VIEW)							
C1+ [1	0	16	V _{CC}				
V+ [2		15	GND				
C1- [3		14	DOUT1				
C2+ [4		13	RIN1				
C2- [5		12	ROUT1				
V- [6		11	DIN1				
DOUT2 [7		10	DIN2				
RIN2]	8		9	ROUT2				

ORDERING INI	FORMATION
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-										
Τ _Α	PACKAG	Eţ	ORDERABLE PART NUMBER	TOP-SIDE MARKING						
		Tube of 40	MAX3232CD	141/20000						
	SOIC (D)	Reel of 2500	MAX3232CDR	MAX3232C						
		Tube of 40	MAX3232CDW							
	SOIC (DW)	Reel of 2000	MAX3232CDWR	MAX3232C						
–0°C to 70°C		Tube of 80	MAX3232CDB	14400000						
	SSOP (DB)	Reel of 2000	MAX3232CDBR	MA3232C						
	TSSOP (PW)	Tube of 90	MAX3232CPW	1400000						
		Reel of 2000	MAX3232CPWR	MA3232C						
		Tube of 40	MAX3232ID							
	SOIC (D)	Reel of 2500	MAX3232IDR	MAX3232I						
		Tube of 40	MAX3232IDW							
-40°C to 85°C	SOIC (DW)	Reel of 2000	MAX3232IDWR	MAX3232I						
		Tube of 80	MAX3232IDB	MD0000						
	SSOP (DB)	Reel of 2000	MAX3232IDBR	MB3232I						
		Tube of 90	MAX3232IPW	MD20201						
	TSSOP (PW)	Reel of 2000	MAX3232IPWR	MB3232I						

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION SLLS410I - JANUARY 2000 - REVISED JANUARY 2004

description/ordering information (continued)

The MAX3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

Function Tables

EACH	DRIVER

INPUT DIN	OUTPUT DOUT			
L	Н			
Н	L			
H = hiah l	evel I = low			

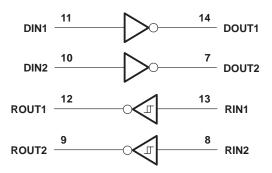
nign ievei, L 10 0 level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT		
L	Н		
н	L		
Open	Н		
H = high level, L = low			

level, Open = input disconnected or connected driver off

logic diagram (positive logic)





MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

SLLS410I - JANUARY 2000 - REVISED JANUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

\mathbf{O} and \mathbf{O} (and \mathbf{N}) (and \mathbf{N})	
	–0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1)	–0.3 V to 7 V
) 0.3 V to –7 V
	–0.3 V to 6 V
	–25 V to 25 V
Output voltage range, V _O : Drivers	–13.2 V to 13.2 V
	-0.3 V to V _{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	: D package
	DB package 82°C/W
	DW package 57°C/W
	PW package 108°C/W
Operating virtual junction temperature, T ₁	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

				MIN	NOM	MAX	UNIT
	Supply veltere		V _{CC} = 3.3 V	3	3.3	3.6	
	Supply voltage		$V_{CC} = 5 V$	4.5	5	5.5	V
	VIH Driver high-level input voltage	DIN	V _{CC} = 3.3 V	2			v
VIH	Driver high-level input voltage	DIN	$V_{CC} = 5 V$	2.4			
VIL	Driver low-level input voltage		DIN			0.8	V
V	Driver input voltage		DIN	0		5.5	M
VI	Receiver input voltage			-25		25	V
-			MAX3232C	0		70	°C
Τ _Α	Operating free-air temperature		MAX3232I	-40		85	-0

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
ICC Supply current	No load, $V_{CC} = 3.3 \text{ V or } 5 \text{ V}$		0.3	1	mA

[‡] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.



MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

SLLS410I - JANUARY 2000 - REVISED JANUARY 2004

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	DOUT at $R_L = 3 k\Omega$ to GND,	DIN = GND	5	5.4		V
VOL	Low-level output voltage	DOUT at $R_L = 3 k\Omega$ to GND,	$DIN = V_{CC}$	-5	-5.4		V
ЧΗ	High-level input current	$V_{I} = V_{CC}$			±0.01	±1	μA
١ _{IL}	Low-level input current	V _I at GND			±0.01	±1	μA
Le et		V _{CC} = 3.6 V,	$V_{O} = 0 V$		105	100	
los‡	Short-circuit output current	V _{CC} = 5.5 V,	$V_{O} = 0 V$	1	±35	±60	mA
r _o	Output resistance	V_{CC} , V+, and V- = 0 V,	$V_{O} = \pm 2 V$	300	10M		Ω

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. [‡] Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Maximum data rate	CL = 1000 pF, One DOUT switching,	RL = 3 kΩ, See Figure 1	150	250		kbit/s
^t sk(p)	Pulse skew§	C _L = 150 pF to 2500 pF	$R_L = 3 k\Omega$ to 7 kΩ, See Figure 2		300		ns
SR(tr)	Slew rate, transition region	$R_L = 3 k\Omega$ to 7 kΩ,	C _L = 150 pF to 1000 pF	6		30	Mue
SK(II)	(see Figure 1)	$V_{CC} = 3.3 V$	$C_{L} = 150 \text{ pF} \text{ to } 2500 \text{ pF}$	4		30	V/μs

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as |tPLH - tPHL| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.



3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15\text{-kV}$ ESD PROTECTION

SLLS410I - JANUARY 2000 - REVISED JANUARY 2004

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	I _{OH} = -1 mA	V _{CC} -0.6V	V _{CC} -0.1 V		V
VOL	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
N/	Desitive raise is suit threads all us the se	V _{CC} = 3.3 V		1.5	2.4	
VIT+	VIT+ Positive-going input threshold voltage	$V_{CC} = 5 V$		1.8	2.4	V
	Manual the sector of the sector back data the sec	$V_{CC} = 3.3 V$	0.6	1.2		
V _{IT} –	Negative-going input threshold voltage	$V_{CC} = 5 V$	0.8	1.5		V
V _{hys}	Input hysteresis (V _{IT+} – V _{IT} _)			0.3		V
ri	Input resistance	$V_{I} = \pm 3 V \text{ to } \pm 25 V$	3	5	7	kΩ

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

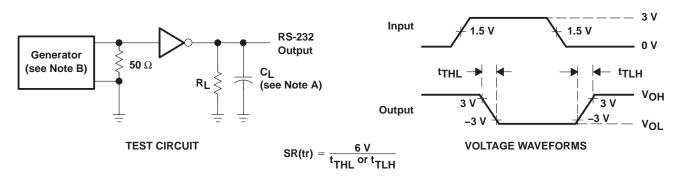
	PARAMETER	TEST CONDITIONS	ΜΙΝ ΤΥΡ [†] ΜΑΧ	UNIT
^t PLH	Propagation delay time, low- to high-level output	0. 450	300	ns
^t PHL	Propagation delay time, high- to low-level output	C _L = 150 pF	300	ns
^t sk(p)	Pulse skew [‡]		300	ns

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡]Pulse skew is defined as |tpLH - tpHL| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_f \le 10$ ns. $t_f \le 10$ ns.

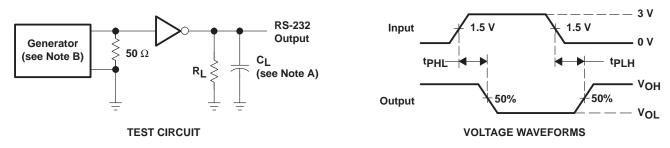
Figure 1. Driver Slew Rate



MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH \pm 15-kV ESD PROTECTION

SLLS410I – JANUARY 2000 – REVISED JANUARY 2004

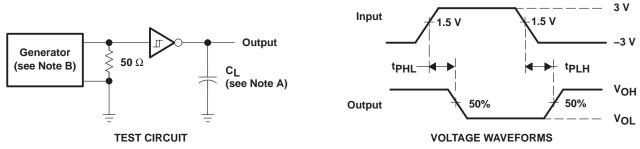
PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_f \le 10$ ns. $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



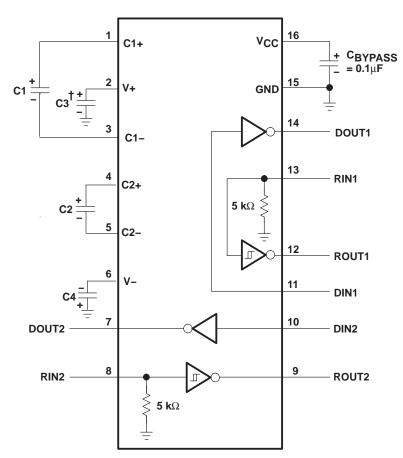
NOTES: A. CL includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times



MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION SLLS410I – JANUARY 2000 – REVISED JANUARY 2004



APPLICATION INFORMATION

- † C3 can be connected to V_CC or GND. NOTES: A. Resistor values shown are nominal.
 - B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

 00		
VCC	C1	C2, C3, C4
.3 V ± 0.3 V 5 V ± 0.5 V 8 V to 5.5 V	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF

V_{CC} vs CAPACITOR VALUES

Figure 4	. Typical	Operating	Circuit and	Capacitor	Values
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TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3232CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

PACKAGE OPTION ADDENDUM

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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3232IDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3232IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



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TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF MAX3232 :

• Enhanced Product: MAX3232-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

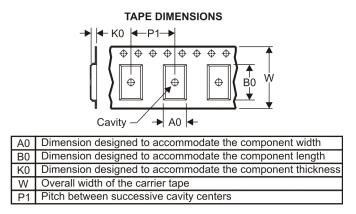
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



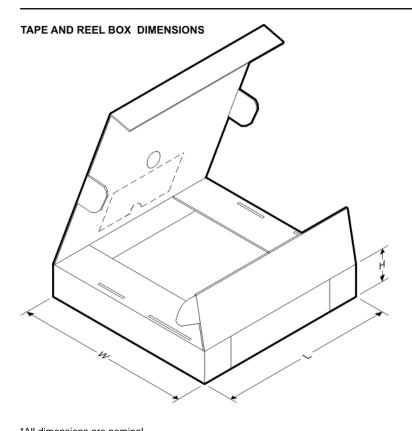
All dimensions are nomina												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3232CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3232CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232CPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
MAX3232CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232IDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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PACKAGE MATERIALS INFORMATION

8-Jul-2011



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3232CDBR	SSOP	DB	16	2000	346.0	346.0	33.0
MAX3232CDWR	SOIC	DW	16	2000	346.0	346.0	33.0
MAX3232CPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
MAX3232CPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
MAX3232IDBR	SSOP	DB	16	2000	346.0	346.0	33.0
MAX3232IDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX3232IDWR	SOIC	DW	16	2000	346.0	346.0	33.0
MAX3232IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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