- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input data is loaded into the master while the clock is high and transferred to the slave and the outputs on the high-tolow clock transistion. For these devices the J and K inputs must be stable while the clock is high.

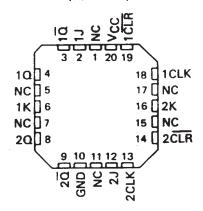
The 'LS107A contain two independent negative-edgetriggered flip-flops. The J and K inputs must be stable prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \overline{Q} output high.

The SN54107 and the SN54LS107A are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74107 and the SN74LS107A are characterized for operation from 0 °C to 70 °C.

SN54107, SN54LS107A J PACKAGE						
SN74107 N PACKAGE						
SN74LS107A D OR N PACKAGE						
(TOP VIEW)						

1341		H VCC
	13	1 1CLR
10[3	12	
1κ[]₄	11]2К
2005	10	2CLR
2 0 [6	9	
	8]2J

SN54LS107A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

	FUNCTION TABLE								
[INPU	TS		OUTF	PUTS				
CLR	CLK	J	к	Q	ā				
L	x	Х	Х	L	н				
н	n	L	L	00	ā0				
н	л	н	L	н	L				
н	л	L	н	L	н				
н	л	н	н	TOG	GLE				

107

'LS107A **FUNCTION TABLE** OUTPUTS INPUTS ā CLR к α CLK J х х L н Ł X ā₀ н L L **Q**0 L н н L H L 1 L н н н ŧ. L н н TOGGLE н £ $\overline{\mathbf{a}}_{\mathbf{0}}$ х х 00 н н

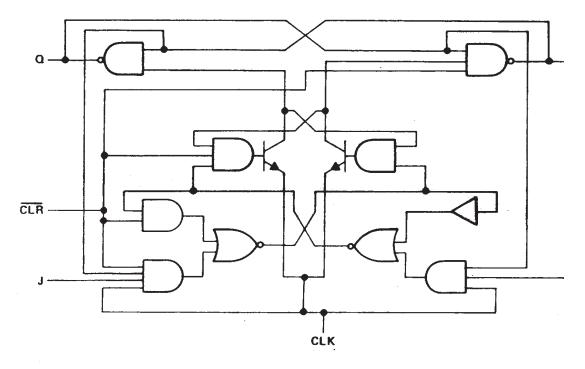
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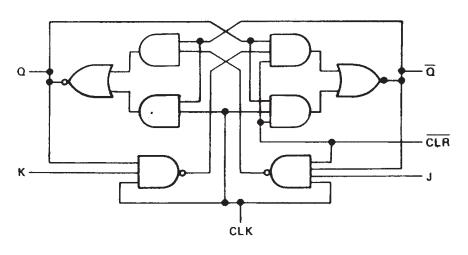


SN54107, SN54LS107A, SN74107, SN74LS107A DUAL J-K FLIP-FLOPS WITH CLEAR SDLS036 – DECEMBER 1983 – REVISED MARCH 1988

logic diagrams (positive logic)

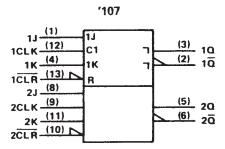


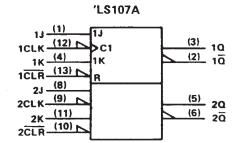






logic symbols[†]



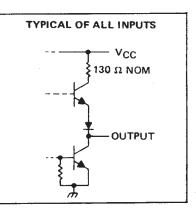


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

schematic of inputs and outputs

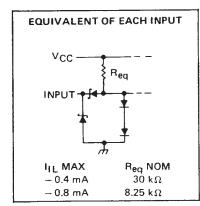
EQUIVALENT OF EACH INPUT

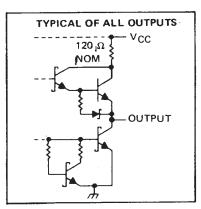
'107



.







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	
Input voltage: '107	5.5 V
	7.
'LS107A	······································
Operating free-air temperature range: SN54'	
SN74'	0°C to 70°C
Storage temperature range	-65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.



SN54107, SN74107 DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS036 - DECEMBER 1983 - REVISED MARCH 1988

recommended operating conditions

				SN54107			SN7410)7	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				- 0.4			- 0.4	mA
10L	Low-level output current	• • • • • • • • •			16			16	mA
		CLK high	20			20			
tw	Pulse duration	CLK low	47	_		47			ns
		CLR low	25			25			
tsu	Input setup time before CLK1		0			0			ns
t _h	Input hold time-data after CLK1		0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS [†]			SN5410	7		7		
	AMETER		TEST CONDITIONS		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = MIN,	l1 = - 12 mA				- 1.5			- 1.5	V
V _{OH}		V _{CC} = MIN, IOH = - 0.4 mA	V _{IH} = 2 V,	V _{1L} = 0.8 V,	2.4	3.4		2.4	3.4		v
VOL		V _{CC} = MIN, I _{OL} = 16 mA	V _{IH} = 2 V,	V _{1L} = 0.8 V,		0.2	0.4		0.2	0.4	v
t _l		V _{CC} = MAX,	V ₁ = 5.5 V	· · _ · _ · _ · _ · · · · · ·			1			1	mA
1	J or K	Vcc = MAX,	V 24 V				40			40	
Чн	All other	VCC - MAA,	V ₁ = 2.4 V				80			80	μA
1	J or K		V - 0.4 V				- 1.6			- 1.6	
ΗL	All other	V _{CC} = MAX,	V ₁ = 0.4 V				- 3.2			- 3.2	mA
los §		V _{CC} = MAX	·		- 20		- 57	- 18		- 57	mA
Icc1	·	V _{CC} = MAX,	See Note 2			10	20		10	20	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25 ° C.

[§]Not more than one output should be shorted at a time.

Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	түр	MAX	UNIT
f _{max}				-	15	20		MHz
^t PLH	CLR	ā	R _L = 400 Ω, C _L = 15 pF			16	25	ns
^t PHL	ULN	Q		С _L ≃ 15 рF		25	40	ns
^t PLH	CLK				16	25	ns	
^t PHL	CLK	0.010				25	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54LS107A, SN74LS107A DUAL J-K FLIP-FLOPS WITH CLEAR

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recommended operating conditions

			S	SN54LS107A MIN NOM MAX		SN74LS107A			UNIT	
			MIN			MIN	NOM	MAX		
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V	
ViH	High-level input voltage		2			2			V	
VIL	Low-level input voltage				0.7			8.0	V	
ЮН	High-level output current			-	- 0.4			- 0.4	mA	
†OL	Low-level output current				4			8	mA	
fclock	Clock frequency		0		30	0		30	MHz	
		CLK high	20			20				
tw	Pulse duration	CLR low	25		;	25			ns	
		data high or low	20			20			-	
tsu	Setup time before CLK I	CLR inactive	25			25			ns	
th	Hold time-data after CLK		0			0			ns	
TA	Operating free-air temperature		- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		-		uct	SN	54LS10	7A	SN	UNIT			
		TEST CONDITIONS [†]		MIN	TYP‡	MAX	MIN	TYP‡		MAX		
Vik		V _{CC} = MIN,	l _l = – 18 mA				- 1.5			- 1.5	V	
v _{он}		V _{CC} = MIN, I _{OH} = 0.4 mA	V _{IH} = 2 V,	VIL = MAX,	2.5	3.4		2.7	3.4		v	
		V _{CC} = MIN, I _{OL} = 4 mA	VIL = MAX,	V _{IH} = 2 V,		0.25	0.4		0.25	0.4	v	
۷OL		V _{CC} = MIN, I _{OL} = 8 mA	V _{IL} = MAX,	V _{IH} = 2 V,					0.35	0.5	•	
	J or K						0.1			0.1		
4	CLR	V _{CC} = MAX,	V1 = 7 V				0.3			0.3	mA	
	CLK						0.4			0.4		
	J or K						20			20		
Чн	CLR	V _{CC} = MAX,	V{ = 2.7 V				60			60	μA	
	CLK						80			80]	
	J or K		N = 0.4 M				- 0.4			- 0.4	mA	
μL	CLR or CLK	V _{CC} = MAX,	V = 0.4 V				- 0.8			- 0.8		
los§		V _{CC} = MAX,	See Note 4		- 20		- 100	- 20		- 100	mA	
ICC (Total)	V _{CC} = MAX,	See Note 2			4	6		4	6	mA	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 \ddagger All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q, outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT
fmax				30	45		MHz
^t PLH		0 5	$R_{L} = 2 k \Omega, \qquad C_{L} = 15$	i pF	15	20	ns
^t PHL	CLR or CLK	Q or Q			15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

9-Oct-2007

PACKAGING INFORMATION

TEXAS INSTRUMENTS www.ti.com

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/00203BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54107J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54107J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN74107N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74107N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74107N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74107N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74107NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74107NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS107AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107AN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS107AN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS107AN3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74LS107AN3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74LS107ANE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
		סוסס	Ν	14	25	Pb-Free	CU NIPDAU	N / A for Pkg Type
SN74LS107ANE4	ACTIVE	PDIP	IN	14	25	(RoHS)	CO NIF DAO	N/AIOII kg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS107ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS107ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54107J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54107J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*A	Il dimensions are nominal												
	Device	•	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	SN74LS107ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
	SN74LS107ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS107ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS107ANSR	SO	NS	14	2000	346.0	346.0	33.0

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless