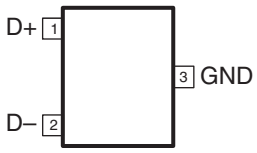
2, 4-CHANNEL PROTECTION SOLUTION FOR SUPER-SPEED (6 GBPS) USB 3.0 INTERFACE

Check for Samples: TPD2EUSB30, TPD2EUSB30A, TPD4EUSB30

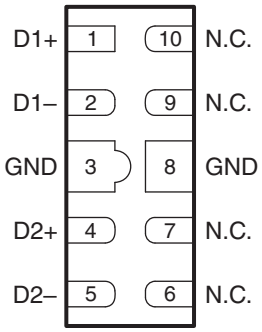
FEATURES

- **Single and Dual-Pair Differential Lines to Protect the Differential Data and Clock Lines of the USB3.0, eSATA, or LVD Interface**
- **Flow-Through Pin Mapping for the High-Speed Lines Ensures near Zero Additional Skew Due to Board Layout While Placing Protection Chip Near the Connector**
- **Supports Data Rates in Excess of 6 Gbps**
- **ESD Protection Meets or Exceeds IEC61000-4-2 (Level 4)**
- **Low Capacitance 0.05pF (IO to IO)**
- **1 Ω Dynamic Resistance**
- **5-A Peak Pulse Current (per 8/20 μs Pulse)**
- **Industrial Temperature Range: –40°C to 85°C**
- **Space-Saving DRT, DQA Packages**

DRT PACKAGE
(TOP VIEW)



DQA PACKAGE
(TOP VIEW)



APPLICATIONS

- **Notebooks**
- **Set-Top Boxes**
- **DVD Players**
- **Media Players**
- **Portable Computers**

DESCRIPTION/ORDERING INFORMATION

The TPD2EUSB30, TPD2EUSB30A, and TPD4EUSB30 provide 2 and 4 channel ESD and surge protection solutions in space saving, flow-through packages. These devices have been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. These devices also offer 5 A (8/20 μs) peak pulse current ratings per IEC 61000-4-5 (lightning) specification.

The monolithic silicon technology allows matching between the differential signal pairs. The differential 0.05-pF capacitance ensures that the signal distortion due to added ESD clamp remains minimal at high-speed differential data transmission.

The TPD2EUSB30A offers low 4.5V dc break-down voltage. The low capacitance and break-down voltage, coupled low dynamic resistance, make the TPD2EUSB30A a superior ESD/ surge protection device for high-speed differential IOs based off ultra-low voltage process nodes.

The TPD2EUSB30 and TPD2EUSB30A are offered in space saving DRT (1 mm × 1 mm) package. The TPD4EUSB30 is offered in space saving DQA (1 mm × 2.5 mm) package. These devices are characterized for operation over ambient air temperature range of –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	SOT – DRT	Tape and reel	TPD2EUSB30DRTR	5P
	SOT – DRT	Tape and reel	TPD2EUSB30ADRTR	5S
	SON – DQA	Tape and reel	TPD4EUSB30DQAR	66_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DQA: The actual top-side marking has one additional character that designates wafer fab/assembly site.

CIRCUIT DIAGRAMS

Figure 1. TPD4EUSB30 Circuit

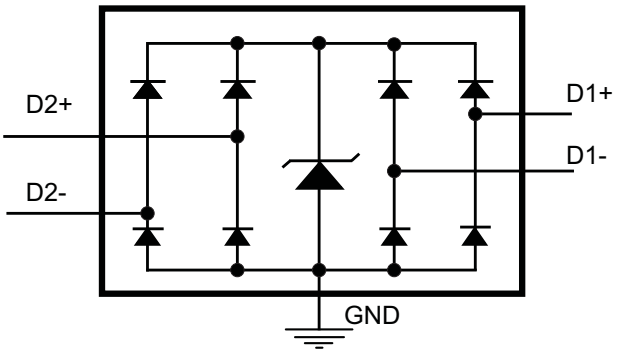
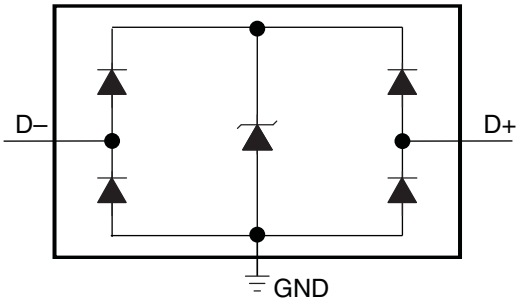


Figure 2. TPD2EUSB30/A Circuit



TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	DRT PIN NO.	DQA PIN NO.		
Dx+, Dx–	1, 2	1,2, 4, 5	ESD port	High-speed ESD clamp, provides ESD protection to the high-speed differential data lines
GND	3	3, 8	GND	Ground
N.C.		6, 7, 9, 10		Not normally connected

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	IO voltage tolerance		D+, D– pins	0	6	
T_A	Operating free-air temperature range			–40	85	°C
T_{stg}	Storage temperature range			–65	125	°C
	ESD protection	IEC 61000-4-2 Contact Discharge	D+, D– pins		±8	kV
		IEC 61000-4-2 Air-Gap Discharge (TPD2EUSB30/A)	D+, D– pins		±8	kV
		IEC 61000-4-2 Air-Gap Discharge (TPD4EUSB30)	D+, D– pins		±9	kV
	Peak pulse current (t_p = 8/20 µs)		D+, D– pins		5	A
	Peak pulse power (t_p = 8/20 µs)		D+, D– pins		45	W

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage, TPD2EUSB30, TPD4EUSB30	D+,D– pins to ground				5.5	V
	Reverse stand-off voltage, TPD2EUSB30A	D+,D– pins to ground				3.6	V
V_{clamp}	Clamp voltage	D+,D– pins to ground,	I_{IO} = 1 A			8	V
I_{IO}	Current from IO port to supply pins	V_{IO} = 2.5 V,	I_D = 8 mA		0.01	0.1	µA
V_D	Diode forward voltage	D+,D– pins, lower clamp diode,	V_{IO} = 2.5 V, I_D = 8 mA	0.6	0.8	0.95	V
R_{dyn}	Dynamic resistance	D+,D– pins	I = 1 A		1		Ω
C_{IO-IO}	Capacitance IO to IO	D+,D– pins	V_{IO} = 2.5 V		0.05		pF
C_{IO-GND}	Capacitance IO to GND	D+,D– pins (DRT)	V_{IO} = 2.5 V		0.7		pF
		D1+, D1-, D2+, D2- (DQA)			0.8		
V_{BR}	Break-down voltage, TPD2EUSB30, TPD4EUSB30	I_{IO} = 1 mA		7			V
	Break-down voltage, TPD2EUSB30A	I_{IO} = 1 mA		4.5			V

TYPICAL OPERATING CHARACTERISTICS

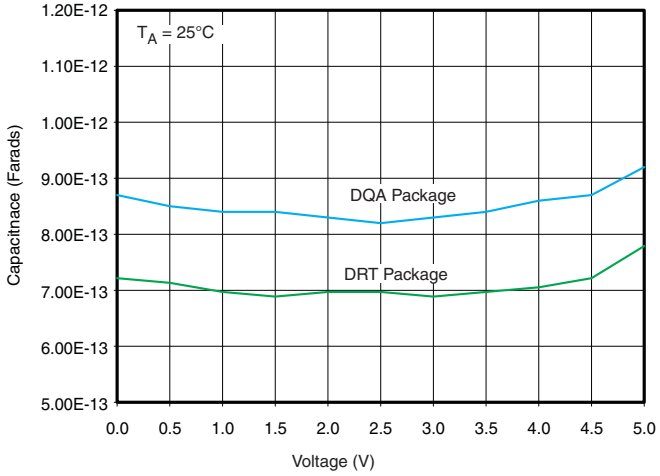


Figure 3. IO Capacitance vs IO Voltage

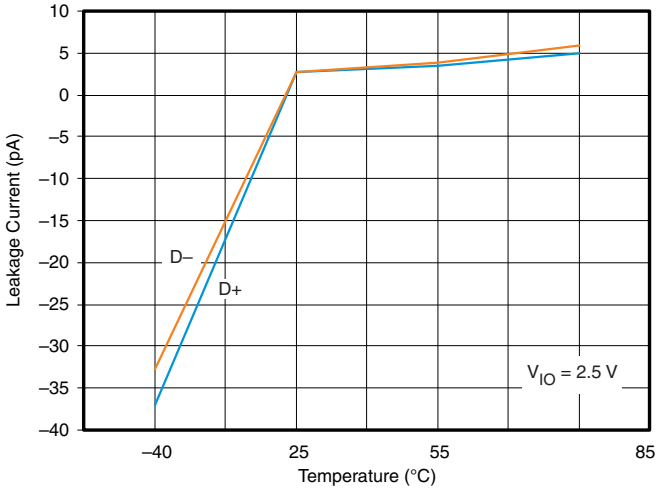


Figure 4. Leakage Current vs Temperature

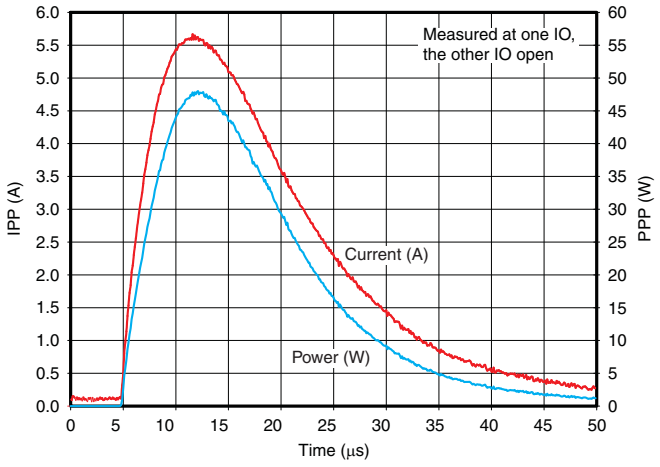


Figure 5. Peak Pulse Waveforms

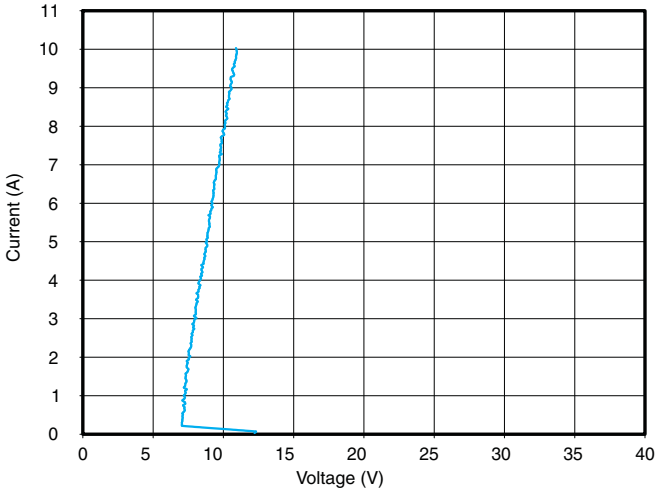


Figure 6. D+,D– Transmission Line Pulser Plot for TPD2EUSB30 (100 ns Pulse, 10 ns Rise Time)

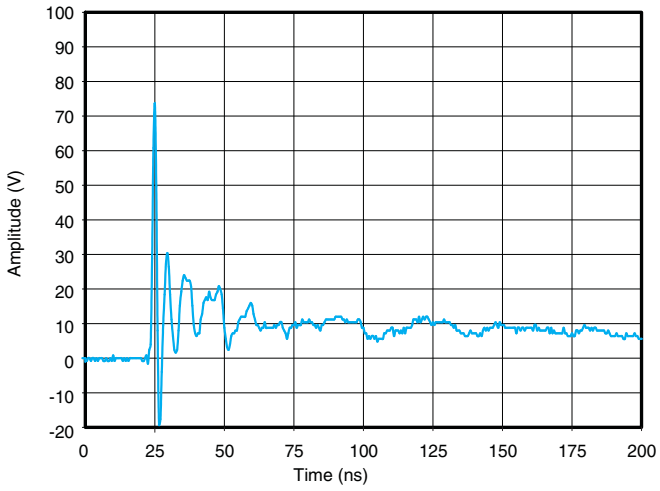


Figure 7. IEC Clamping Waveforms (8 kV Contact)

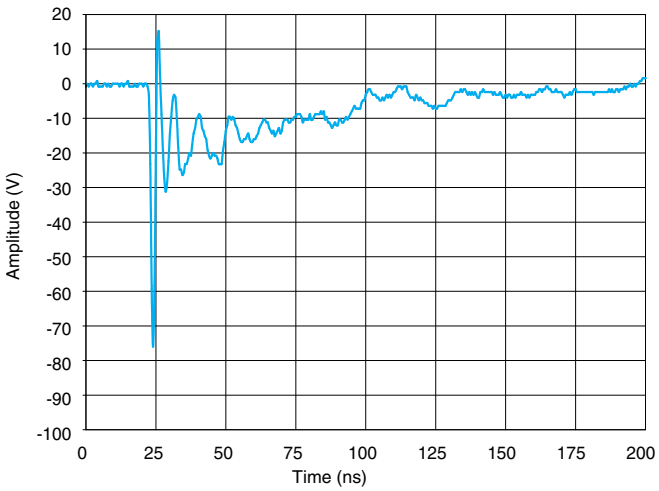


Figure 8. IEC Clamping Waveforms (–8 kV Contact)

TYPICAL OPERATING CHARACTERISTICS (continued)

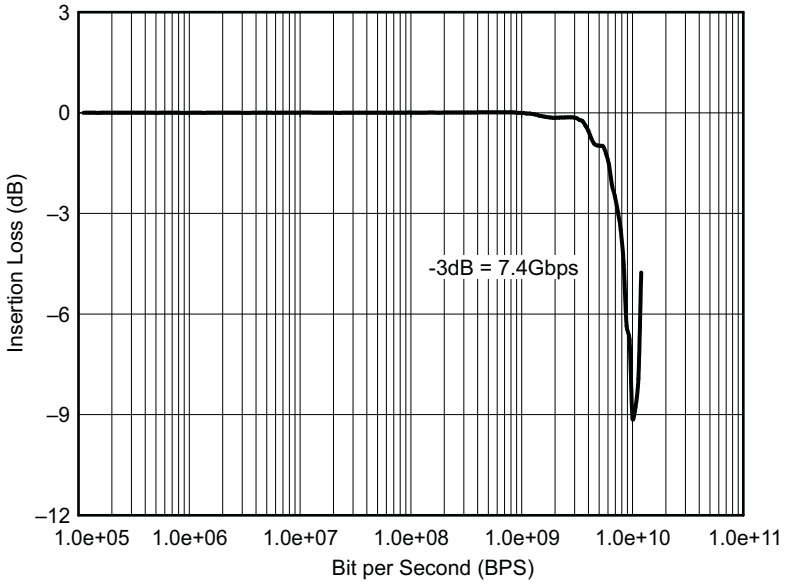


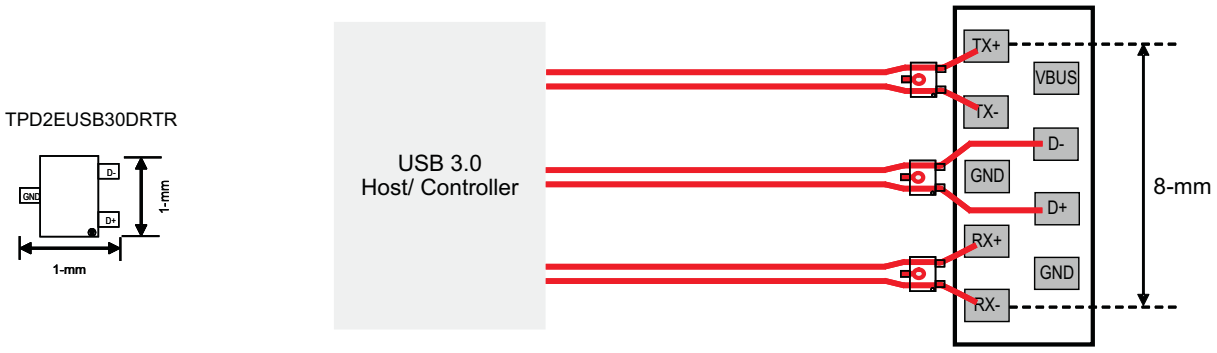
Figure 9. Insertion Loss

APPLICATION INFORMATION

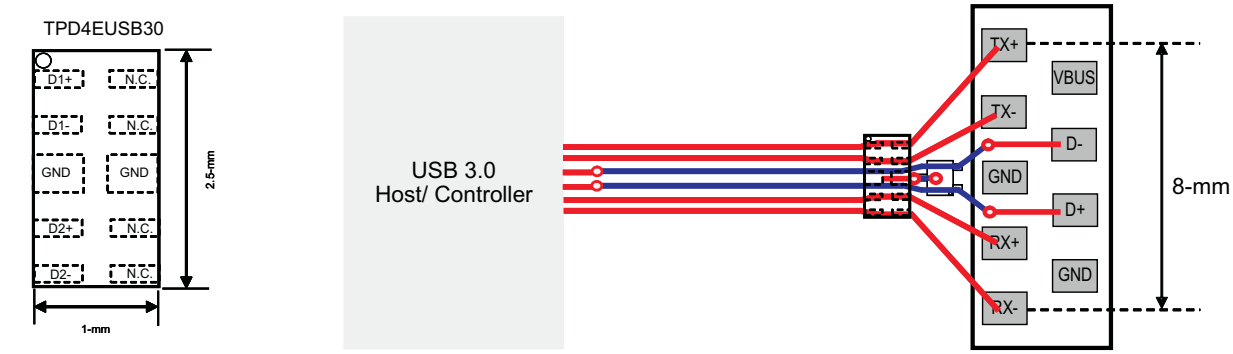
Layout Guide with TPDxEUSB30/A

Refer to Figure 10, the TPD2EUSB30/A are offered in space saving DRT package. The DRT is a 1mm* 1mm package with flow-through pin-mapping for the high-speed differential lines. The TPD4EUSB30 is offered in space saving DQA package. The DQA is a 1mm* 2.5mm package with flow-through pin-mapping for the high-speed differential lines. It is recommended to place the package right next to the USB 3.0 connector. The GND pin should connected to GND plane of the board through a large VIA. If a dedicated GND plane is not present right underneath, it is recommended to route to the GND plane through a wide trace. The current associated with IEC ESD stress can be in the range of 30Amps or higher momentarily. A good, low impedance GND path ensures the system robustness against IEC ESD stress.

The TPDxEUSB30/A can provide system level ESD protection to the high-speed differential ports (>6 Gbps data rate). The flow-through package offers flexibility for board routing with traces up to 15 mills wide. It allows the differential signal pairs couple together right after they touch the ESD ports of the TPDxEUSB30/A.



Three TPD2EUSB30 to Protect USB3.0 Class A connector (One Layer Routing)



One TPD4EUSB30 & One TPD2EUSB30 to Protect USB3.0 Class A connec tor (Two Layer Routing)

Figure 10. Layout Guide with the TPDxEUSB30/A at the USB3.0 Class A Connector

TPDxEUSB30/A Eye Pattern Test

See Figure 12 for a demonstration of the TPDxEUSB30/A performance the lab set-up. Figure 11 shows a lab board that was designed to demonstrate the degradation of the eye pattern quality with and without the TPD2EUSB30/A in the USB 3.0 signal path. Figure 13 shows that there is only ~2 ps jitter penalty to the differential signal when the TPD2EUSB30/A device was added in the signal path. Similar setup was employed to measure eye pattern for the TPD4EUSB30.

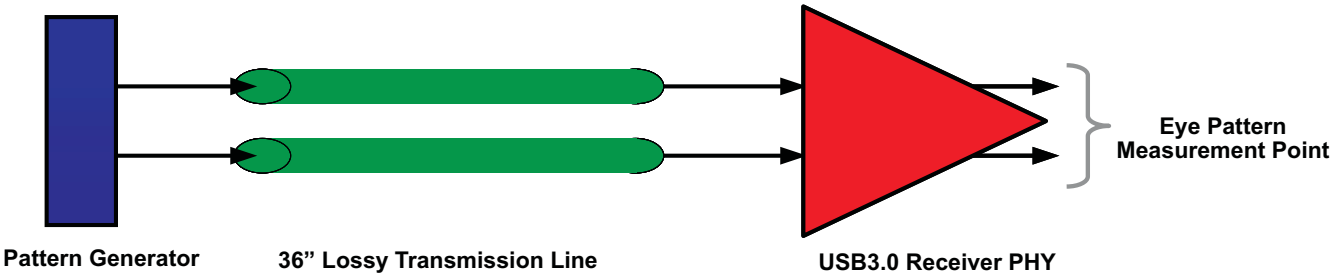


Figure 11. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30/A

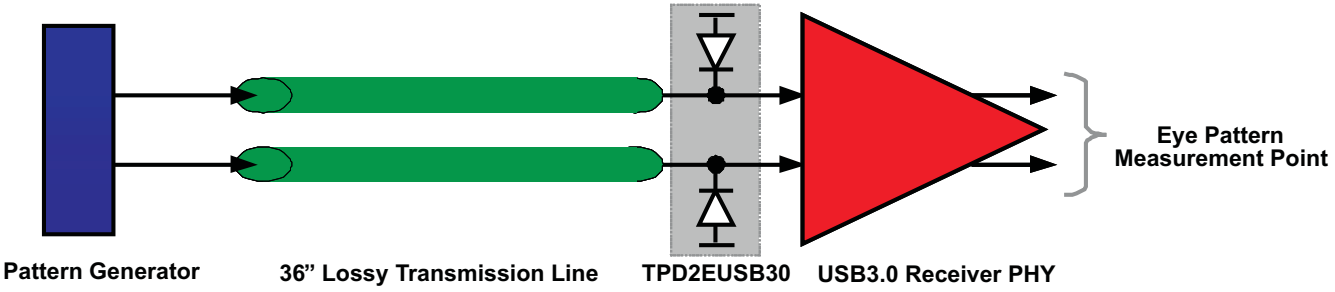


Figure 12. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30/A

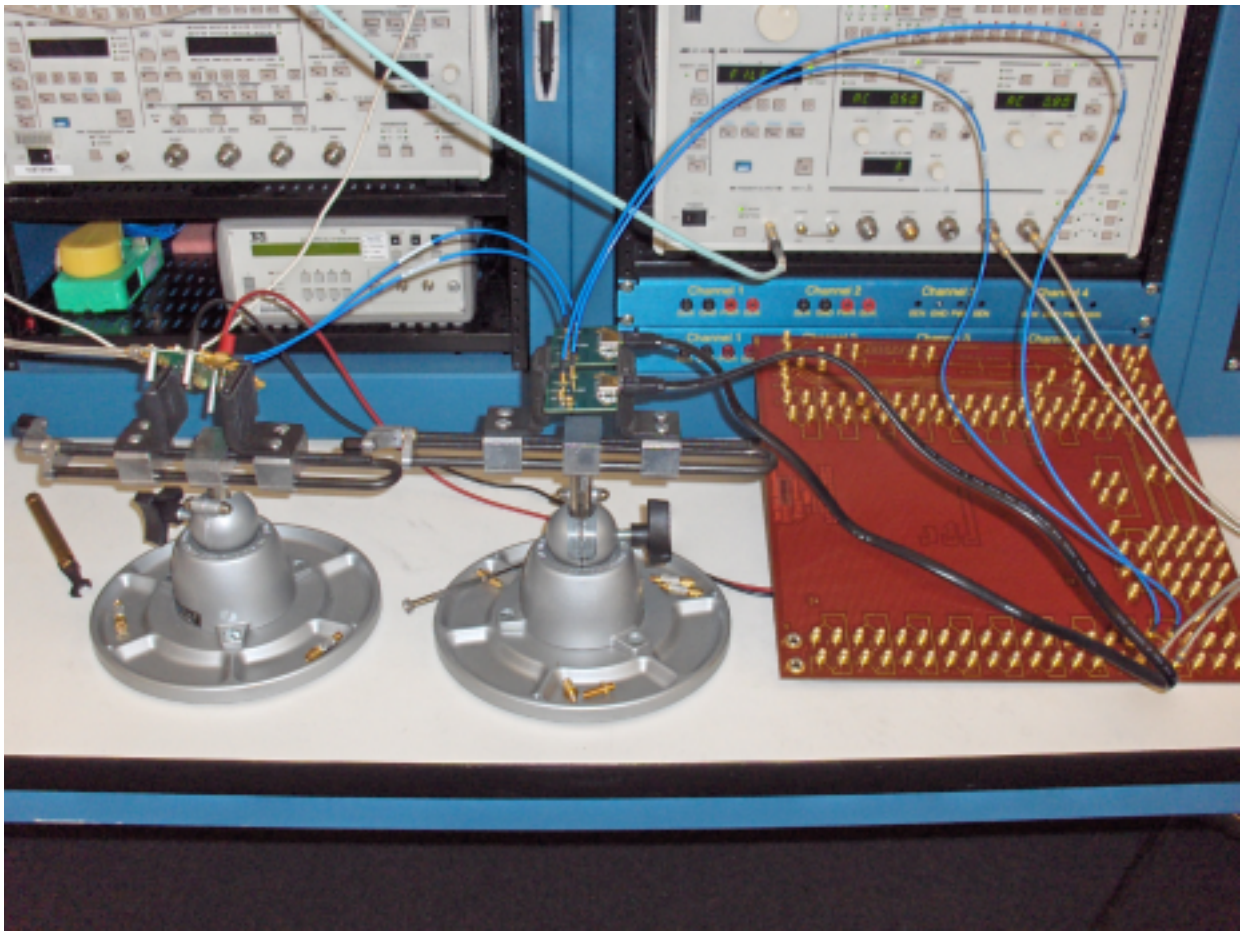


Figure 13. Lab Setup for the Eye-Pattern Measurement with TPDxEUSB30/A

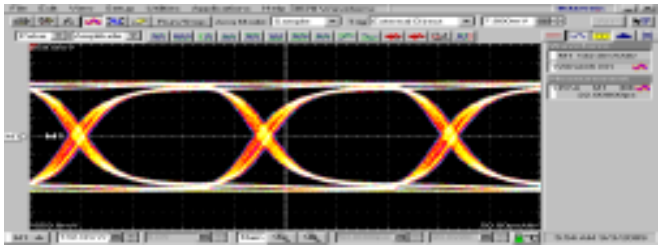


Figure 14. Output Eye Diagram Without TPD2EUSB30/A (Figure 11 Setup, 5 Gbps Data Rate)

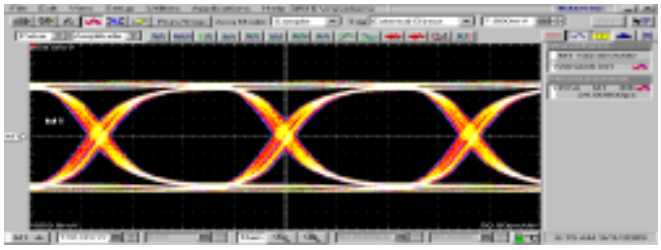


Figure 15. Output Eye Diagram with the TPD2EUSB30/A (Figure 11 Setup, 5 Gbps Data Rate)

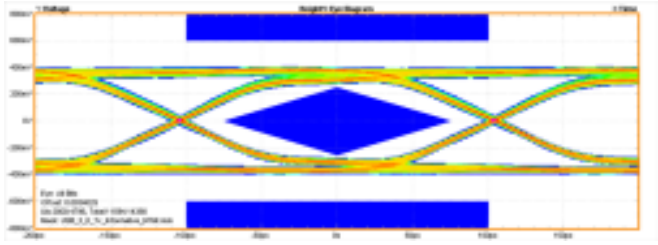


Figure 16. Output Eye Diagram Without the TPD4EUSB30 (5 Gbps Data Rate)

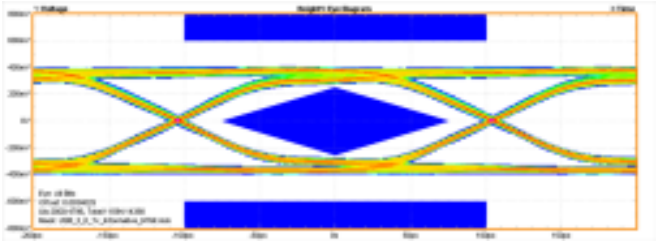


Figure 17. Output Eye Diagram with the TPD4EUSB30 (5 Gbps Data Rate)

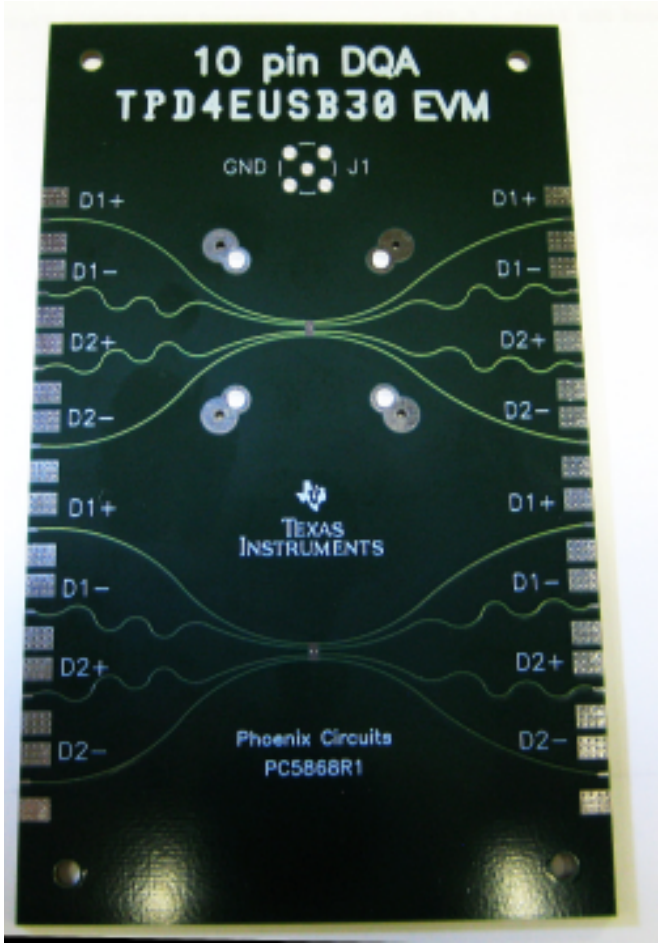


Figure 18. TPDxEUSB30/A EVM – TPD4EUSB30 Side

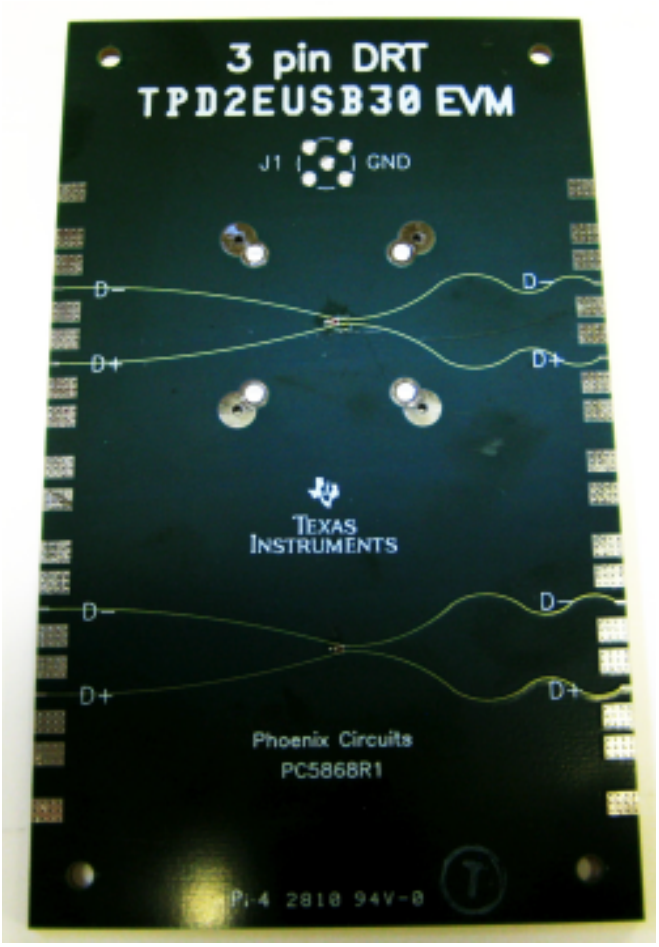


Figure 19. TPDxEUSB30/A EVM – TPD2EUSB30/A Side

REVISION HISTORY

Changes from Original (August 2010) to Revision A	Page
• Added TPS2EUSB30A part to document.	1

Changes from Revision A (December 2010) to Revision B	Page
• Changed TOP-SIDE MARKING column in the Ordering Information Table.	2

Changes from Revision B (July 2011) to Revision C	Page
• Added Insertion Loss graphic to TYPICAL OPERATING CHARACTERISTICS section.	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPD2EUSB30ADRTR	ACTIVE	SOT	DRT	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPD2EUSB30DRTR	ACTIVE	SOT	DRT	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPD4EUSB30DQAR	ACTIVE	SON	DQA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

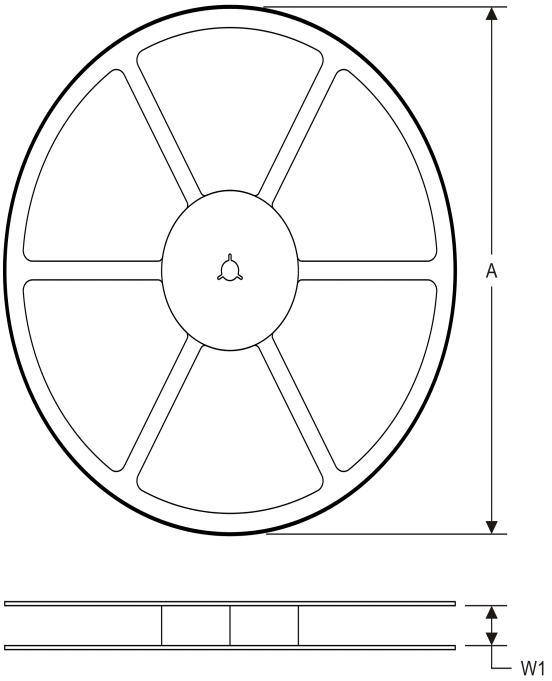
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

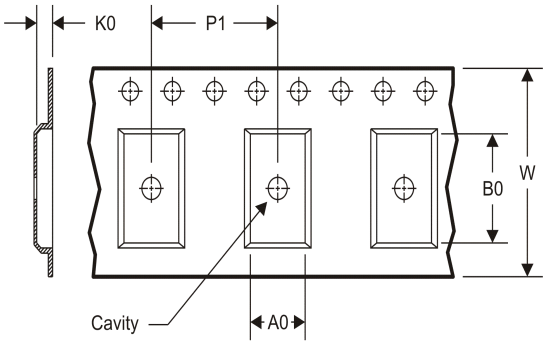
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



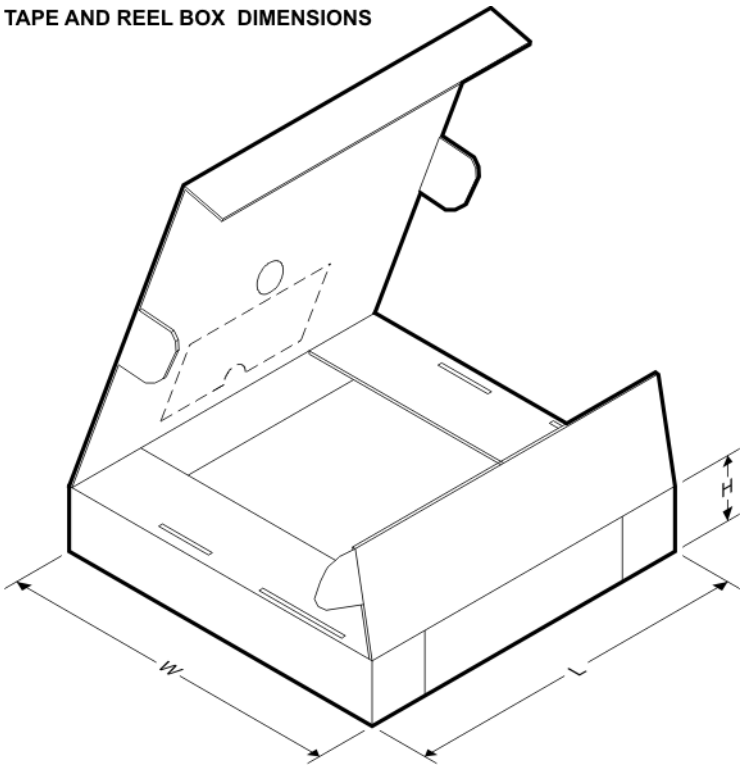
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

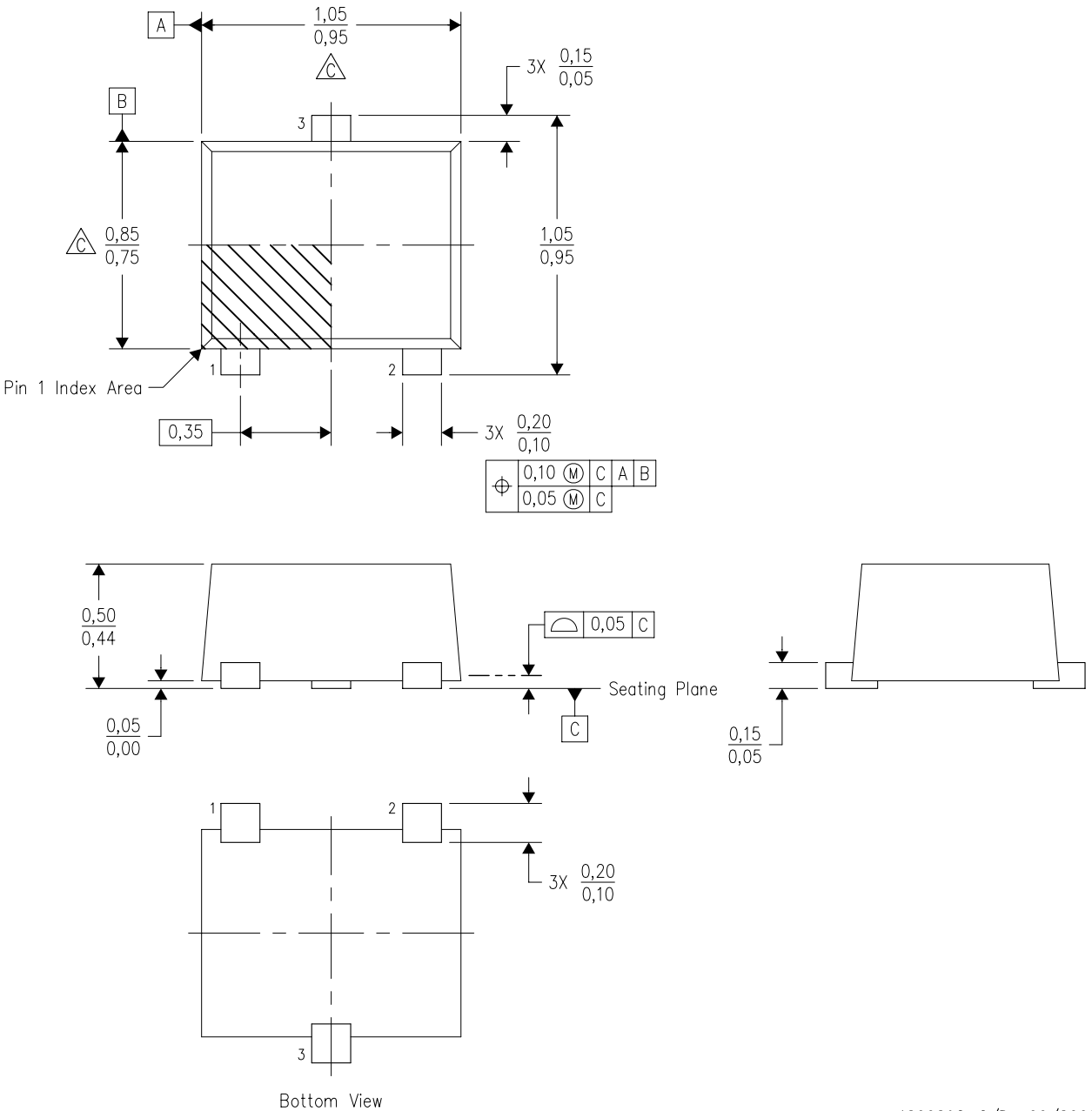
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2EUSB30ADRTR	SOT	DRT	3	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
TPD2EUSB30DRTR	SOT	DRT	3	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



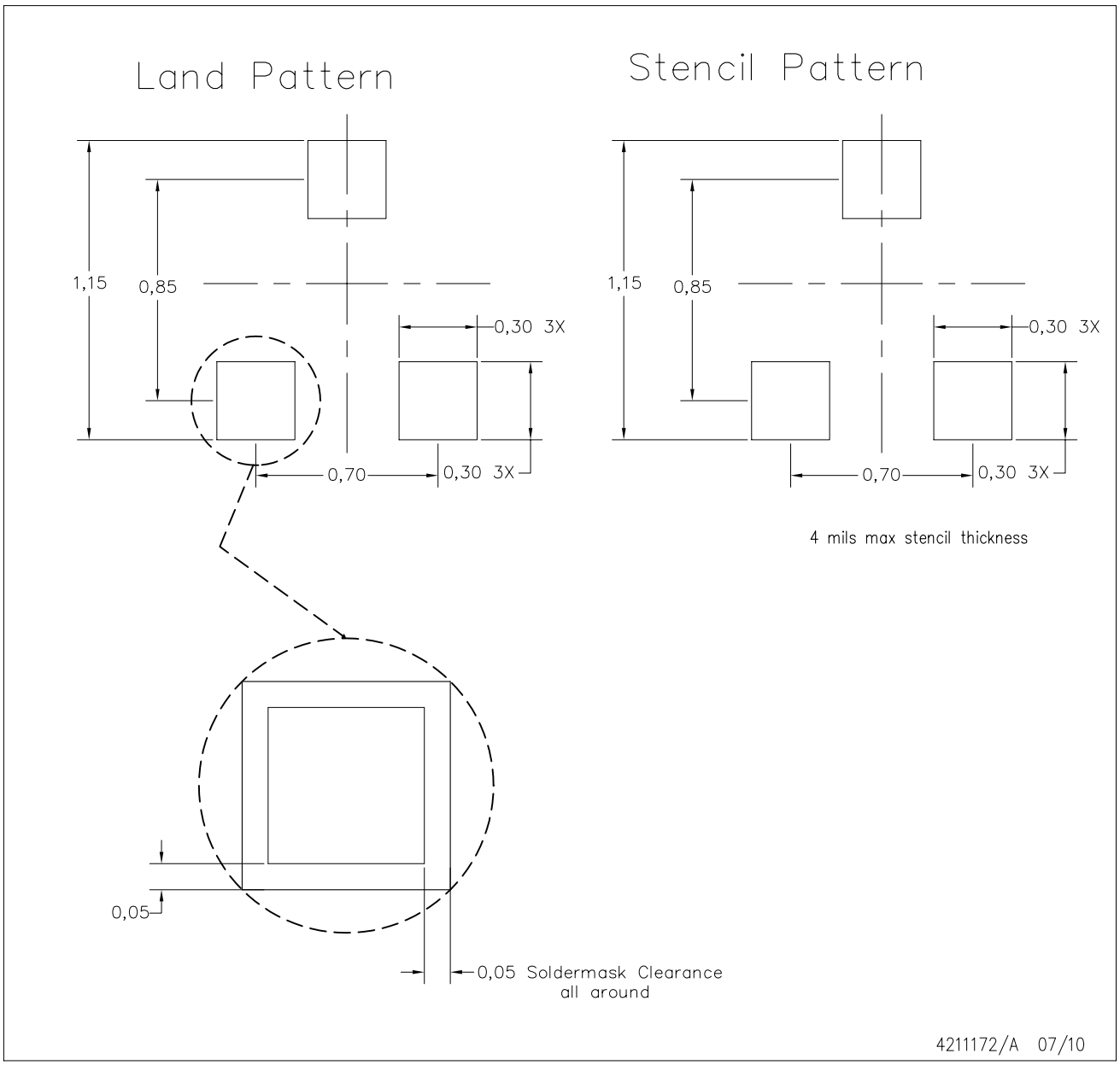
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2EUSB30ADRTR	SOT	DRT	3	3000	202.0	201.0	28.0
TPD2EUSB30DRTR	SOT	DRT	3	3000	202.0	201.0	28.0



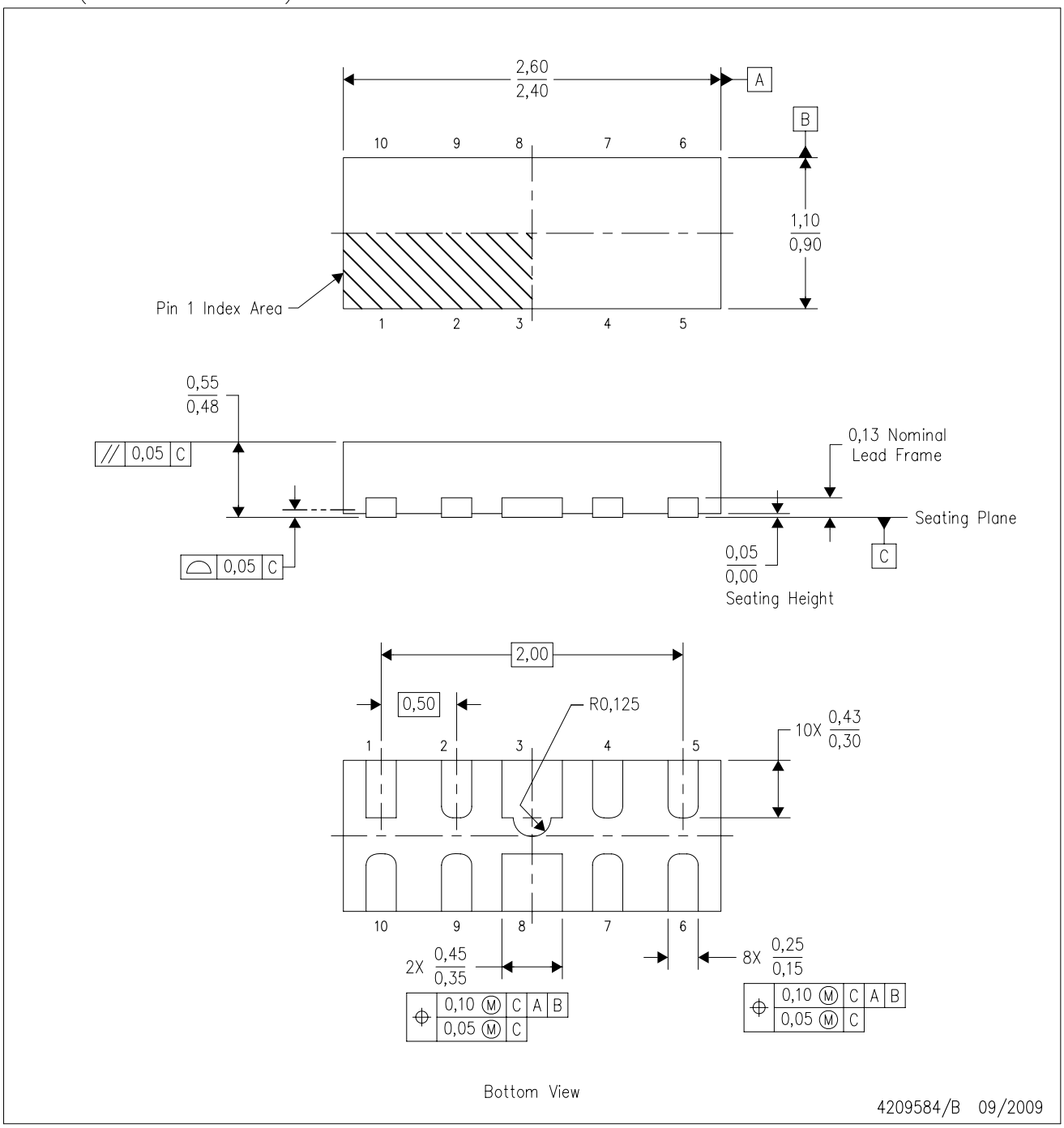
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
D. JEDEC package registration is pending.

DRT (S–PDSO–N3) PLASTIC SMALL OUTLINE



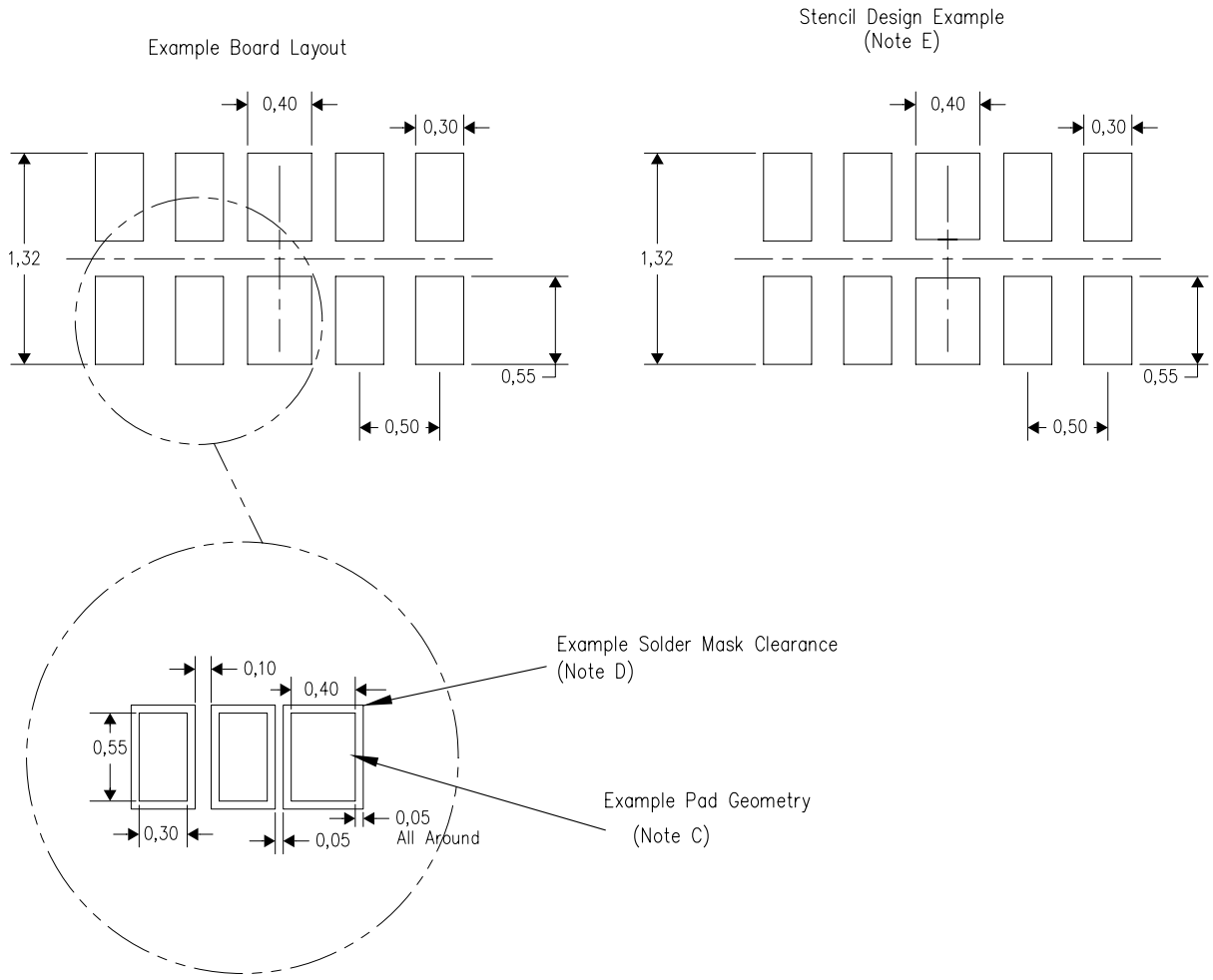
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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