

MSP430F22x2/22x4 Device Erratasheet

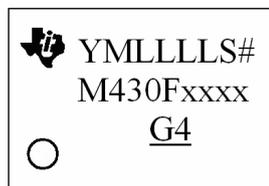
Current Version

Devices	Rev:	BCL12	PORT10	TA12	TA16	TB2	TB16	USCI20	XOSC5
MSP430F2232	F	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	F	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	F	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	F	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	F	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	F	✓	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

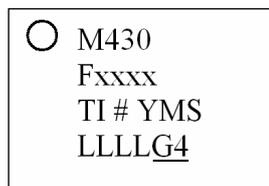
Package Markings

DA38: TSSOP(DA) 38-pin



YM = Year and Month Date Code
 LLLL = LOT Trace Code
 S = Assembly Site Code
 # = DIE Revision
 o = PIN 1

RHA40: QFN(RHA) 40-pin



YM = Year and Month Date Code
 LLLL = LOT Trace Code
 S = Assembly Site Code
 # = DIE Revision
 o = PIN 1

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Detailed Bug Description

BCL12 BCL12 - Bug description:

Module: BasicClock, Function: Switching RSEL can cause DCO dead time

After switching RSELx bits (located in register BCCTL1) from a value of >13 to a value of <12, the resulting clock delivered by the DCO can stop for a certain time before the new clock frequency gets applied. This dead time is in the range of 20 μ s.

Workaround:

Use an intermediate step when switching RSEL from >13 to <12. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

PORT10 Port10 - Bug description:

Module: Digital I/O, Function: Pullup/pulldown resistor selection when module pin function is selected

When the pullup/pulldown resistor for a certain port pin is enabled (PxREN.y=1) and the module port pin function is selected (PxSEL.y=1), the pullup/pulldown resistor configuration of this pin is controlled by the respective module output signal (Module X OUT) instead of the port output register (PxOUT.y).

Workaround:

None. Do not set PxSEL.y and PxREN.y at the same time.

TA12 TA12 - Bug description:

Module: Timer_A, Function: Interrupt is lost (slow ACLK)

Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

Detailed Bug Description (continued)

TA16 TA16 - Bug description:

Module: Timer_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:

None

TB2 TB2 - Bug description:

Module: Timer_B, Function: Interrupt is lost (slow ACLK)

Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if TBR = CCRx + 1). This interrupt gets lost.

Workaround:

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TB16 TB16 - Bug description:

Module: Timer_B, Function: First increment of TBR erroneous when IDx > 00

The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

Workaround:

None

Detailed Bug Description (continued)

USCI20 USCI20 - Bug description:

Module: USCI, Function: I2C Mode Multi-master transmitter issue

When configured for I2C master-transmitter mode, and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following four conditions are true:

1. Two masters are generating SCL
and
2. The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA
and
3. The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line gets released
and
4. The transmit buffer has not been loaded before the other master continues communication by driving SCL low

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI will interfere with the current bus activity and may cause unpredictable bus behavior.

Workaround:

1. Ensure that slave doesn't stretch the SCL low phase of an ACK period
or
2. Ensure that the transmit buffer is loaded in time
or
3. Do not use the multi-master transmitter mode

XOSC5 XOSC5 - Bug description:

Module: LFXT1 OSC, Function: LF crystal failures may not be properly detected by the oscillator fault circuitry

The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU; i.e., OFIFG will not be set.

Workaround:

None

Appendix: Prior Versions

Devices	Rev:	BCL12	CPU14	FLASH21	FLASH22	JTAG13	JTAG14	PORT10	TA12	TA16	TB2	TB16	USCI16	USCI20	XOSC5
MSP430F2232	F	✓						✓	✓	✓	✓	✓		✓	✓
	E	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	F	✓						✓	✓	✓	✓	✓		✓	✓
	E	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	F	✓						✓	✓	✓	✓	✓		✓	✓
	E	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	F	✓						✓	✓	✓	✓	✓		✓	✓
	E	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	F	✓						✓	✓	✓	✓	✓		✓	✓
	E	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	F	✓						✓	✓	✓	✓	✓		✓	✓
	E	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Detailed Bug Description

CPU14 CPU14 - Bug description:

Module: CPU, Function: Erroneous setting of SCG0 after reset

The SCG0 bit in the CPU status register (SR) is set after any reset (PUC or POR) if bit 6 in the reset vector destination address is set. Setting SCG0 turns off the DCO DC generator when DCOCLK is not used for MCLK or SMCLK.

Workarounds:

- As the error only occurs after PUC or POR, it is sufficient to clear the SCG0 bit at the beginning of the program code. Example:

```
bic.w #SCG0, SR
```
- Avoid using reset destination addresses where bit 6 is set. Allowed reset vector destination addresses are xx0xh, xx1xh, xx2xh, xx3xh, xx8xh, xx9xh, xxAxh, and xxBxh.

When any of the above reset destination addresses are used, SCG0 is valid.

FLASH21 FLASH21 - Bug description:

Module: Flash, Function: Info memory read data corrupted

Flash addresses between 0x1080 and 0x10ff (information memory) might not be read correctly. Supply voltages and addressing mode affect the read value.

Workaround:
None

Detailed Bug Description (continued)

FLASH22 FLASH22 – Bug description

Module: Flash, Function: Flash controller may prevent correct LPM entry

When ACLK (or SMCLK) is used as the Flash controller clock source, and this clock source gets deactivated due to a low-power mode entry while a Flash erase or write operation is pending, the Flash controller will keep ACLK (or SMCLK) active even after the Flash operation has been completed. This will result in an incorrect LPM entry and increased current consumption. Note that this issue can only occur when the Flash operation and the low-power mode entry are initiated from code located in RAM.

Workaround:

Do not enter low-power modes while Flash erase or write operations are active. Wait for the operation to be completed before entering a low-power mode.

JTAG13 JTAG13 - Bug description:

Module: JTAG, Function: PSA Checksum generation fails

PSA checksum generation gives a wrong result when data_psa is executed during test clock low phase and last address of FLASH info memory addresses 0x107e or 0x10fe are part of the calculation.

Workaround:

Calculate PSA sum when test clock is at high level.

JTAG14 JTAG14 - Bug description:

Module EEM, Function: Releasing JTAG control can corrupt CPU registers during debug

During a debug session, on rare occasions, the CPU register contents can get corrupted when JTAG control is released by the debugger. This behavior is exhibited during, but not limited to, the use of the “Use Virtual Breakpoints” and “Force Single Stepping” features in the IAR Embedded Workbench software. This bug does not affect normal device and application operation, such as starting a device out of POR and executing application code.

In order for the bug to occur, both of the following two conditions must be true:

1. The CPU (MCLK) is sourced by the DCO
and
- 2 The “External Resistor (Rosc)” feature of the DCO is not used

Workaround:

Use an external crystal or a digital high-speed clock source connected to the LFXT1 oscillator to source the CPU (MCLK) during a debug session. Alternatively, use the on-chip DCO in the “External Resistor (Rosc)” configuration. Note that, in this case, an external resistor connected to the device’s Rosc pin is mandatory, and that the factory-programmed DCO calibration constants cannot be applied directly.

Detailed Bug Description (continued)

USCI16 USCI16 - Bug description:

Module: USCI, Function: UART/IrDA mode lost characters

When configured for UART/IrDA mode, the USCI baud rate generator may halt operation under the following conditions:

1. IrDA mode: Repeated invalid start bits on the receive line

or

2 .UART/IrDA modes: Positive pulse on the receive line during break character reception inside the stop-bit time slot (the second stop-bit time slot in case of UCSPB = 1) with a pulse width that passes the deglitch filter but is shorter than half a bit time.

After halting, additional characters will be ignored. Transmit functionality is not affected.

Workaround:

Check the UCBUSY flag status periodically in software. If the flag is set and no character has been received in the expected time, reset the USCI module in software. To reset the USCI module, toggle UCSWRST and reenale the USCI interrupts.

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