3-Channel, 12-Bit, PWM Constant-Current LED Driver with Single-Wire Interface (EasySet™)

Check for Samples: TLC5973

FEATURES

- **Three Constant Sink Current Channels**
- **Current Capability:**
  - **2 mA to 35 mA per Channel (VCC ≤ 4.0 V)**
  - **2 mA to 50 mA per Channel (VCC > 4.0 V)**
- **Grayscale (GS) Control with PWM:**
  - **12-Bit (4096 Steps)**
- **Single-Wire Interface (EasySet)**
- **Power-Supply (VCC) Voltage Range:**
  - **3 V to 6 V**
- **OUT Terminals Maximum Voltage: Up to 21 V**
- **Integrated Shunt Regulator**
- **Data Transfer Maximum Rate:**
  - **Bits per Second (bps): 3 Mbps**
- **Internal GS Clock Oscillator: 12 MHz (typ)**
- **Display Repeat Rate: 2.9 kHz (typ)**
- **Output Delay Switching to Prevent Inrush Current**
- **Unlimited Device Cascading**
- **Operating Temperature: –40°C to +85°C**

APPLICATIONS

- **RGB LED Cluster Lamp Display**

DESCRIPTION

The TLC5973 is an easy-to-use, 3-channel, 50-mA constant sink current LED driver. The single-wire, 3-Mbps serial interface (EasySet) provides a solution for minimizing wiring cost. The LED driver provides 8-bit pulse width modulation (PWM) resolution. The display repeat rate is achieved at 2.9 kHz (typ) with an integrated 12-MHz grayscale (GS) clock oscillator. The driver also provides unlimited cascading capability.

All output sink constant currents can be set by an external resistor. The TLC5973 has an internal shunt regulator that can be used for higher VCC power-supply voltage applications.

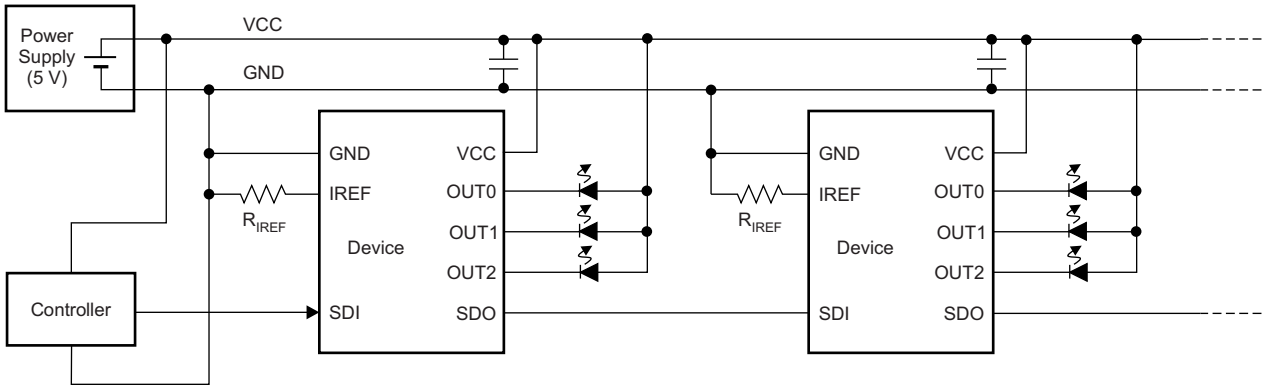


Figure 1. Typical Application Circuit Example 1 (No Internal Shunt Regulator Mode)

DESCRIPTION (CONTINUED)

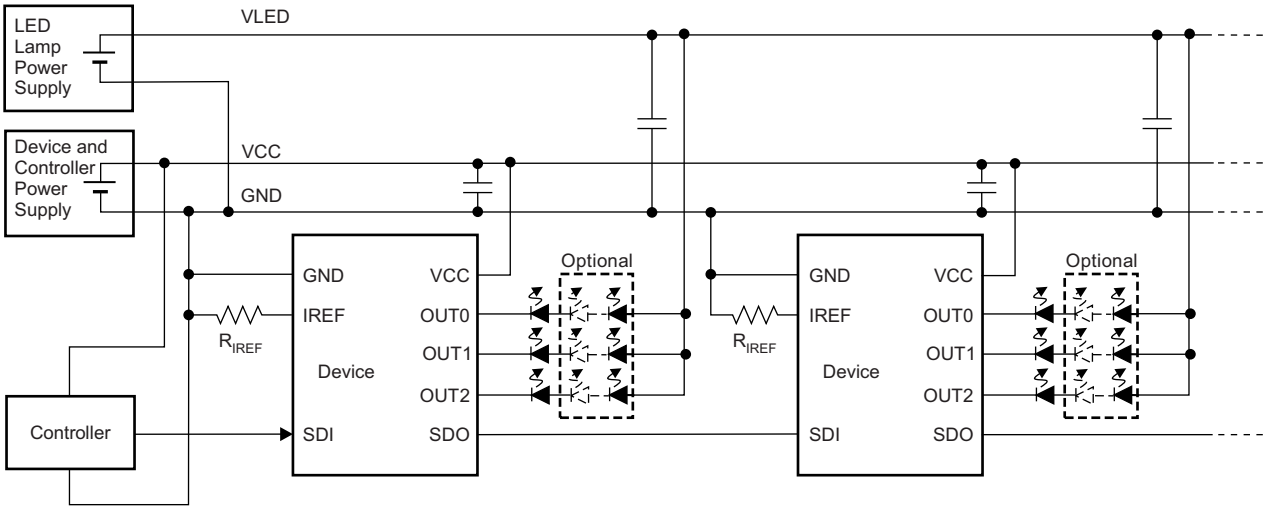


Figure 2. Typical Application Circuit Example 2 (No Internal Shunt Regulator Mode)

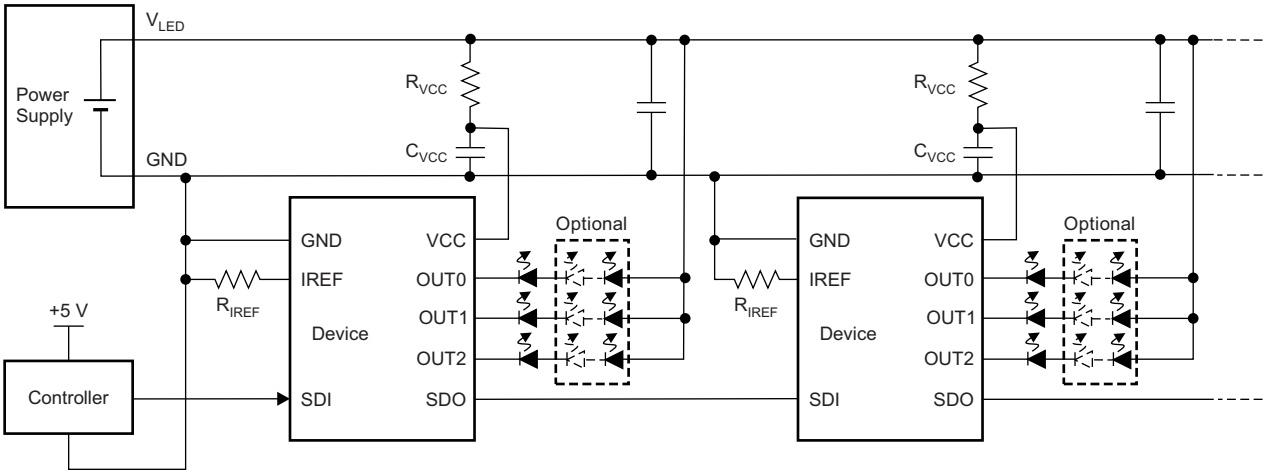


Figure 3. Typical Application Circuit Example 3 (Internal Shunt Regulator Mode)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA
TLC5973	SO-8	TLC5973DR	Tape and Reel
		TLC5973D	Tube

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
Voltage(2)	Supply, V_{CC}	VCC	–0.3	+7.0	V
	Input range, V_{IN}	SDI	–0.3	V_{CC} + 1.2	V
	Output range, V_{OUT}	OUT0 to OUT2	–0.3	+21	V
		SDO	–0.3	+7.0	V
Current	Output (dc), I_{OUT}	OUT0 to OUT2	0	+60	mA
Temperature	Operating junction, T_J		–40	+150	°C
	Storage, T_{stg}		–55	+150	°C
Electrostatic discharge (ESD) ratings:	Human body model (HBM)			8000	V
	Charged device model (CDM)			2000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC5973 D (SO) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	134.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	88.6	
θ_{JB}	Junction-to-board thermal resistance	75.3	
ψ_{JT}	Junction-to-top characterization parameter	37.7	
ψ_{JB}	Junction-to-board characterization parameter	74.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply voltage	No internal shunt regulator mode	3.0	5.0	5.5	V
		Internal shunt regulator mode			6.0	V
V_O	Voltage applied to output	OUT0 to OUT2			21	V
V_{IH}	High-level input voltage	SDI	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SDI	GND		0.3 × V_{CC}	V
V_{IHYST}	Input voltage hysteresis	SDI		0.2 × V_{CC}		V
I_{OH}	High-level output current	SDO			–2	mA
I_{OL}	Low-level output current	SDO			2	mA
		OUT0 to OUT2 (VCC ≤ 4.0 V)	2		35	mA
		OUT0 to OUT2 (VCC > 4.0 V)	2		50	mA
I_{REG}	Shunt regulator sink current	VCC			20	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC CHARACTERISTICS						
$f_{CLK\ (SDI)}$	Data transfer rate	SDI	100		3000	kHz
t_{SDI}	SDI input pulse duration	SDI	60		0.5 / f_{CLK}	ns
t_{WH}	Pulse duration, high	SDI	14			ns
t_{WL}	Pulse duration, low	SDI	14			ns
t_{H0}	Hold time: end of sequence (EOS)	SDI↑ to SDI↑	3.5 / f_{CLK}		5.5 / f_{CLK}	µs
t_{H1}	Hold time: data latch (GSLAT)	SDI↑ to SDI↑	8 / f_{CLK}			µs

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3 V to 6.0 V, and C_{VCC} = 0.1 µF. Typical values at T_A = +25°C and V_{CC} = 5.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (SDO)	I_{OH} = –2 mA		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage (SDO)	I_{OL} = 2 mA		0		0.4	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.5 kΩ		1.18	1.20	1.23	V
V_R	Shunt regulator output voltage (V_{CC})	I_{CC} = 1 mA, SDI = low			5.9		V
I_{CC0}	Supply current (V_{CC})	V_{CC} = 3.0 V to 5.5 V , SDI = low, all grayscale (GS*n*) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 27 kΩ (I_{OUTn} = 2-mA target)			3	6	mA
I_{CC1}		V_{CC} = 3.0 V to 5.5 V, SDI = low, all grayscale (GS*n*) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 3 kΩ (I_{OUTn} = 17-mA target)			4	7	mA
I_{CC2}		V_{CC} = 3.0 V to 5.5 V, SDI = 5 MHz, all grayscale (GS*n*) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 3 kΩ (I_{OUTn} = 17-mA target)			5	8	mA
I_{CC3}		V_{CC} = 3.0 V to 5.5 V, SDI = 5 MHz, all grayscale (GS*n*) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 1.5 kΩ (I_{OUTn} = 34-mA target)			5.5	10	mA
I_{OLC}	Constant output current (OUT0 to OUT2)	All OUT*n* = on, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ		31	34	37	mA
I_{OLKG}	Output leakage current (OUT0 to OUT2)	GS*n* = 000h, V_{OUTn} = 21 V	T_J = –40°C to +85°C			0.1	µA
			T_J = +85°C to +125°C			0.2	µA
ΔI_{OLC0}	Constant-current error (channel-to-channel)(1)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5%	±3%	
ΔI_{OLC1}	Constant-current error (device-to-device)(2)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5%	±6%	
ΔI_{OLC2}	Line regulation of constant-current output(3)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5	±1	%/V
ΔI_{OLC3}	Load regulation of constant-current output(4)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5	±1	%/V
R_{PD}	Internal pull-down resistance (SDI)	At SDI			1		MΩ

(1) The deviation of each output (OUT0 to OUT2) from the constant-current average. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\frac{I_{OUT0} + I_{OUT1} + I_{OUT2}}{3}} - 1 \right) \times 100$$

where n = 0 to 2.

(2) Deviation of the constant-current average in each color group from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{\frac{I_{OUT0} + I_{OUT1} + I_{OUT2}}{3} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUTn(IDEAL)}\,(\text{mA}) = 43.4 \times \left(\frac{1.20}{R_{IREF}\,(\Omega)} \right)$$

where n = 0 to 2.

(3) Line regulation is calculated by the formula:

$$\Delta\,(\%/\text{V}) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}{I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V}} \right) \times \frac{100}{5.5\text{ V} - 3.0\text{ V}}$$

where n = 0 to 2.

(4) Load regulation is calculated by the equation:

$$\Delta\,(\%/\text{V}) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0\text{ V})}{I_{OUTn} \text{ at } V_{OUTn} = 1.0\text{ V}} \right) \times \frac{100}{3.0\text{ V} - 1.0\text{ V}}$$

where n = 0 to 2.

SWITCHING CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3.0 V to 5.5 V, C_L = 15 pF, R_L = 110 Ω, and V_{LED} = 5.0 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 5.0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SDO	2	6	12	ns
t_{R1}		OUT*n* (on → off)		200	400	ns
t_{F0}	Fall time	SDO	2	6	12	ns
t_{F1}		OUT*n* (off → on)		200	400	ns
t_{D0}	Propagation delay	SDI↑ to SDO↑		30	50	ns
t_{D1}		OUT0↓ to OUT1↓, OUT1↓to OUT2↓, OUT0↑ to OUT1↑, OUT1↑to OUT2↑		25		ns
t_{WO}	Shift data output one pulse duration	SDO↑ to SDO↓	15	25	45	ns
f_{OSC}	Internal GS oscillator frequency		8	12	16	MHz

PARAMETER MEASUREMENT INFORMATION

PIN-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

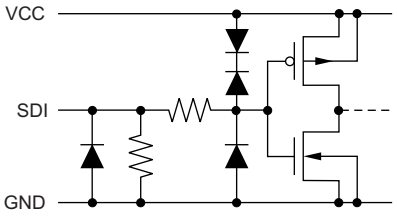


Figure 4. SDI

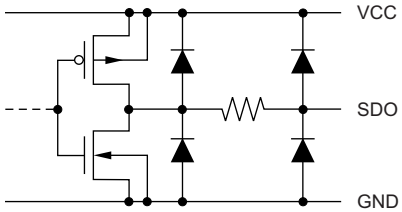
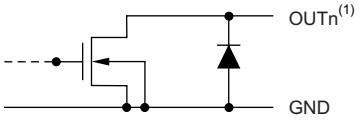


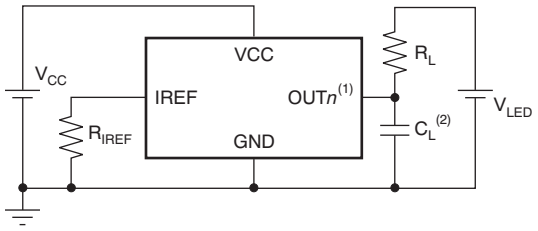
Figure 5. SDO



(1) n = 0 to 2.

Figure 6. OUT0 Through OUT2

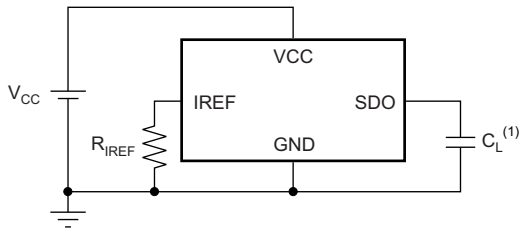
TEST CIRCUITS



(1) n = 0 to 2.

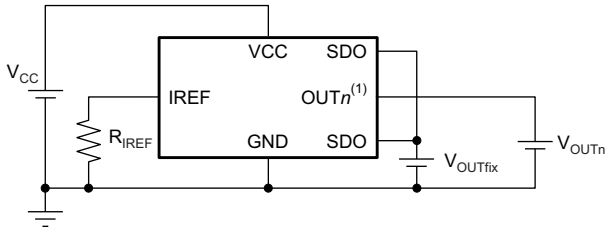
(2) C_L includes measurement probe and jig capacitance.

Figure 7. Rise Time and Fall Time Test Circuit for OUT*n*



(1) C_L includes measurement probe and jig capacitance.

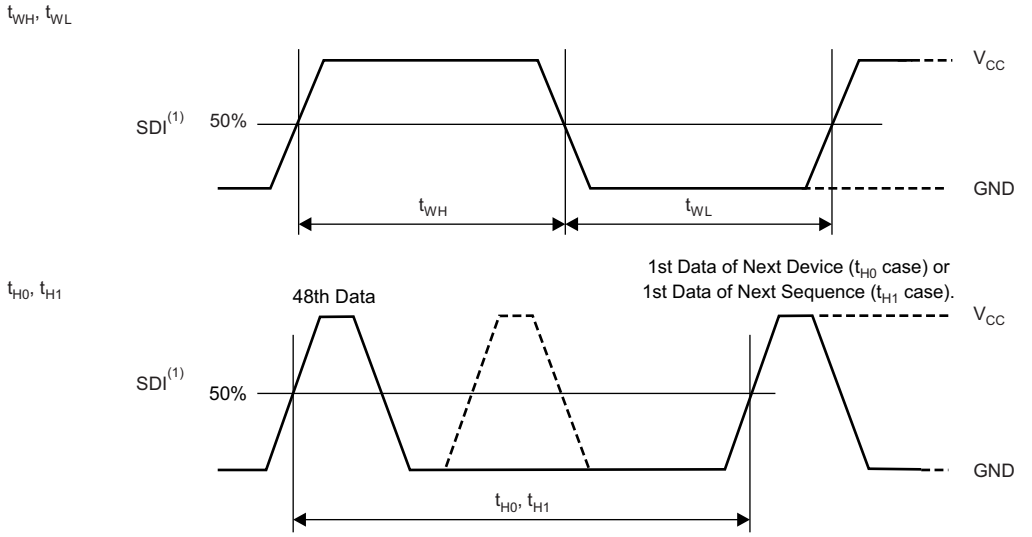
Figure 8. Rise Time and Fall Time Test Circuit for SDO



(1) n = 0 to 2.

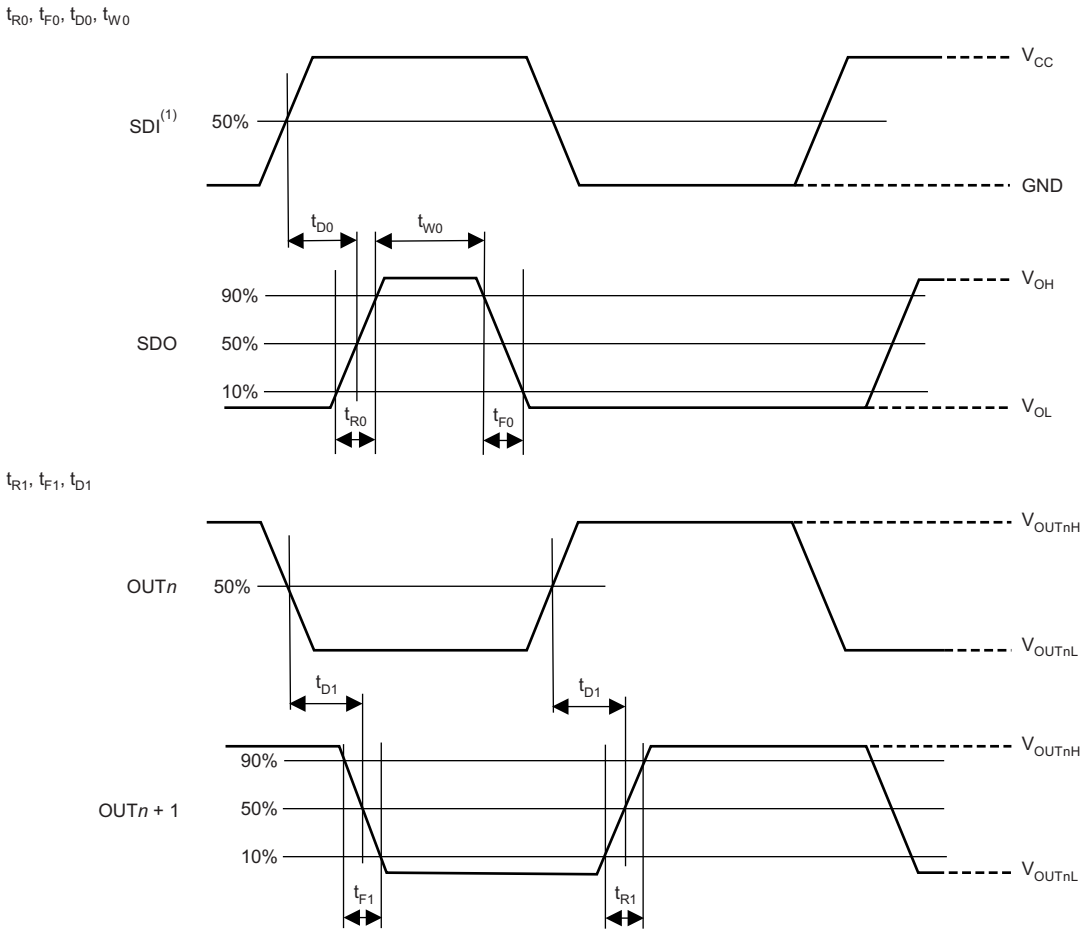
Figure 9. Constant-Current Test Circuit for OUT*n*

TIMING DIAGRAMS



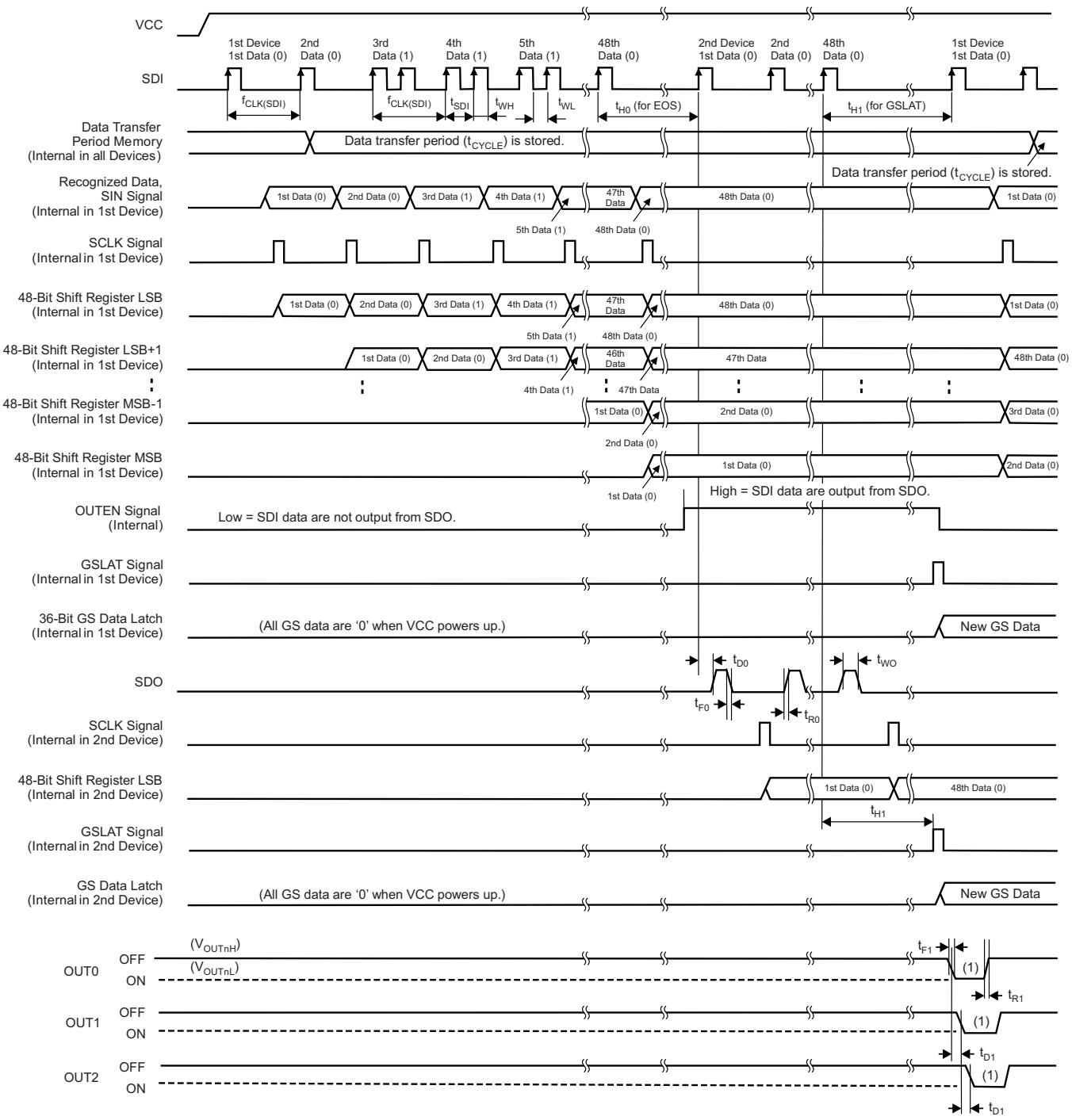
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 10. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 11. Output Timing

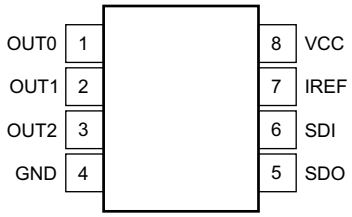


(1) OUT*n* on-time changes, depending on the data in the 36-bit GS data latch.

Figure 12. Data Write and OUT*n* Switching Timing

PIN CONFIGURATION

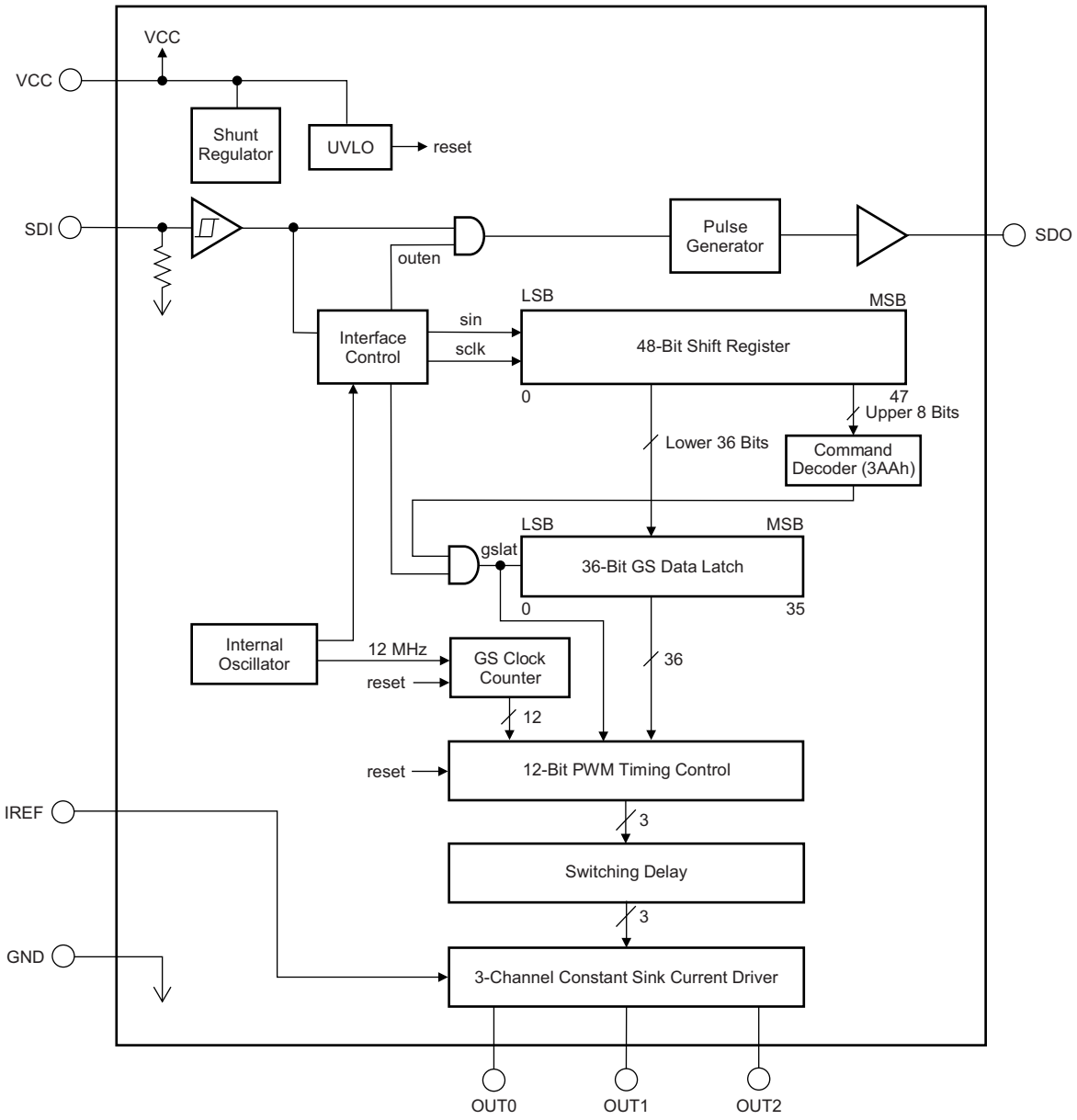
D PACKAGE
SO-8
(Top View)



PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	4	—	Power ground
IREF	7	I/O	Output current programming terminal. A resistor connected between IREF and GND sets the current for each constant-current output. Place the external resistor close to the device.
OUT0	1	O	Constant sink current driver outputs. Multiple outputs can be configured in parallel to increase the sink drive current capability. Different voltages can be applied to each output.
OUT1	2	O	
OUT2	3	O	
SDI	6	I	Serial data input. This pin is internally pulled down to GND with a 1-MΩ (typ) resistor.
SDO	5	O	Serial data output
VCC	8	—	Power-supply voltage

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = 12 V, unless otherwise noted.

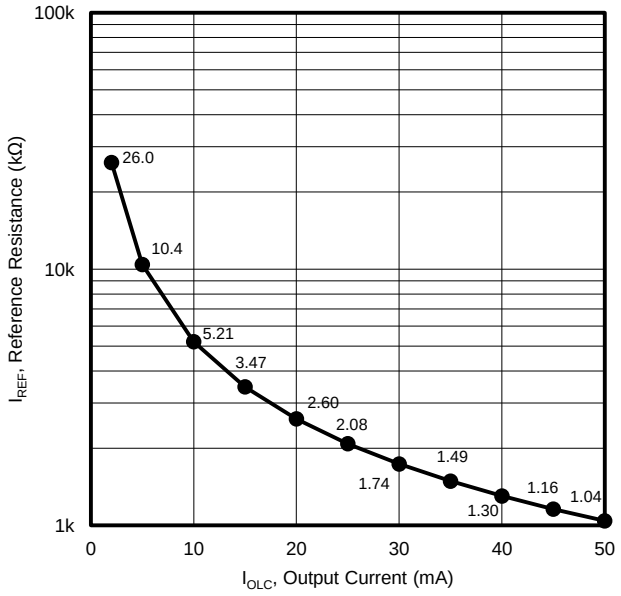


Figure 13. REFERENCE RESISTOR vs OUTPUT CURRENT (OUT*n*)

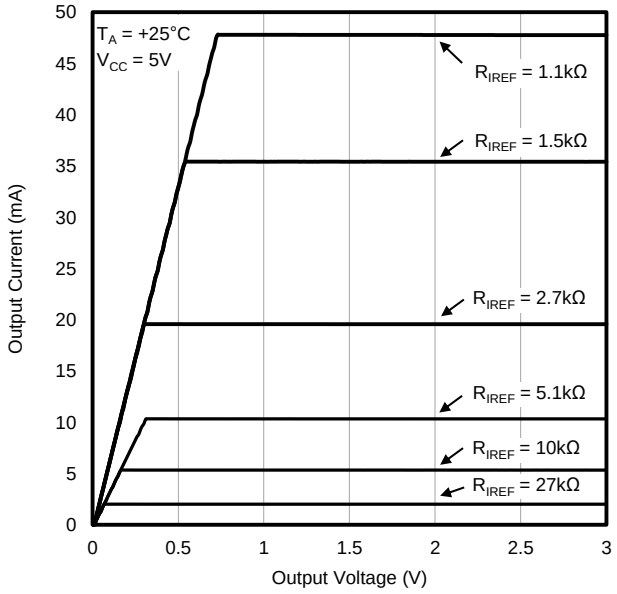


Figure 14. OUTPUT CURRENT vs OUTPUT VOLTAGE (OUT*n*)

DETAILED DESCRIPTION

CONSTANT SINK CURRENT VALUE

The output current value of each channel (I_{OLC}) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by Equation 1:

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \times 43.4 \quad (1)$$

where:

- V_{IREF} = the internal reference voltage on IREF (typically 1.20 V), and
- I_{OLC} = 2 mA to 50 mA

I_{OLC} is the current for each output. Each output sinks I_{OLC} current when it is turned on. R_{IREF} must be between 1 kΩ and 27 kΩ in order to hold I_{OLC} between 50 mA (typ) and 1.93 mA (typ). Otherwise, the output may be unstable. Refer to Figure 13 and Table 1 for the constant-current sink values for specific external resistor values.

Table 1. Constant-Current Output versus External Resistor Value

I_{OLC} (mA)	R_{IREF} (kΩ, typ)
50	1.04
45	1.16
40	1.30
35	1.49
30	1.74
25	2.08
20	2.60
15	3.47
10	5.21
5	10.4
2	26.0

RESISTOR AND CAPACITOR VALUE SETTING FOR SHUNT REGULATOR

The TLC5973 internally integrates a shunt regulator to regulate V_{CC} voltage. Refer to Figure 15 for an application circuit that uses the internal shunt regulator through a resistor, R_{VCC}. The recommended R_{VCC} value can be calculated by Equation 2.

$$\frac{V_{LED}\,(V) - 5.9\ V}{13\ mA} < R_{VCC} < \frac{V_{LED}\,(V) - 5.9\ V}{11\ mA} \quad (2)$$

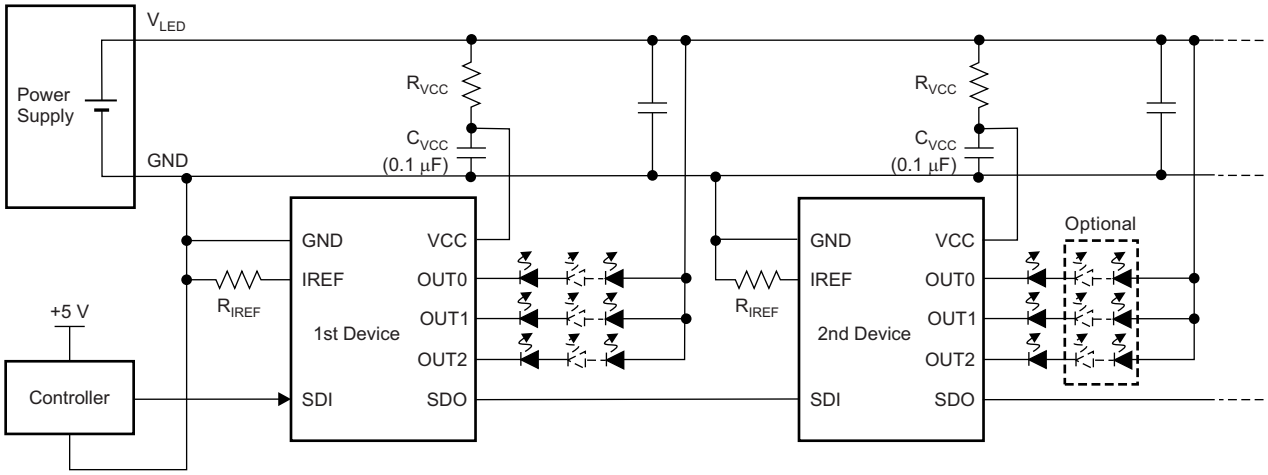


Figure 15. Internal Shunt Regulator Mode Application Circuit

Table 2 shows the typical resistor value for several V_{LED} voltages. Note that the C_{VCC} value should be 0.1 µF.

Table 2. Resistor Example for Shunt Resistor versus LED Voltage(1)

V_{LED} (V)	R_{VCC} (Ω)	RESISTOR WATTAGE (W)
9	390	0.03
12	820	0.07
18	1500	0.15
24	2200	0.21

(1) R_{IREF} is at 1.5 kΩ.

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The TLC5973 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The PWM data bit length for each output is 12 bits. The architecture of 12 bits per channel results in 4096 brightness steps, from 0% to 99.98% on-time duty cycle.

The PWM operation for OUT*n* is controlled by an 12-bit grayscale (GS) counter. The GS counter increments on each internal GS clock (GSCLK) rising edge. All OUT*n* are turned on when the GS counter is '1'. All OUT*n* turn on when the GS count is '1', except when OUT*n* are programed to GS data '0' in the 36-bit GS data latch. After turning on, each output is turns off when the GS counter value exceeds the programmed GS data for the output. The GS counter resets to 00h and all outputs are forced off when the GS data are written to the 36-bit GS data latch. Afterwards, the GS counter begins incrementing and PWM control is started from the next internal GS clock.

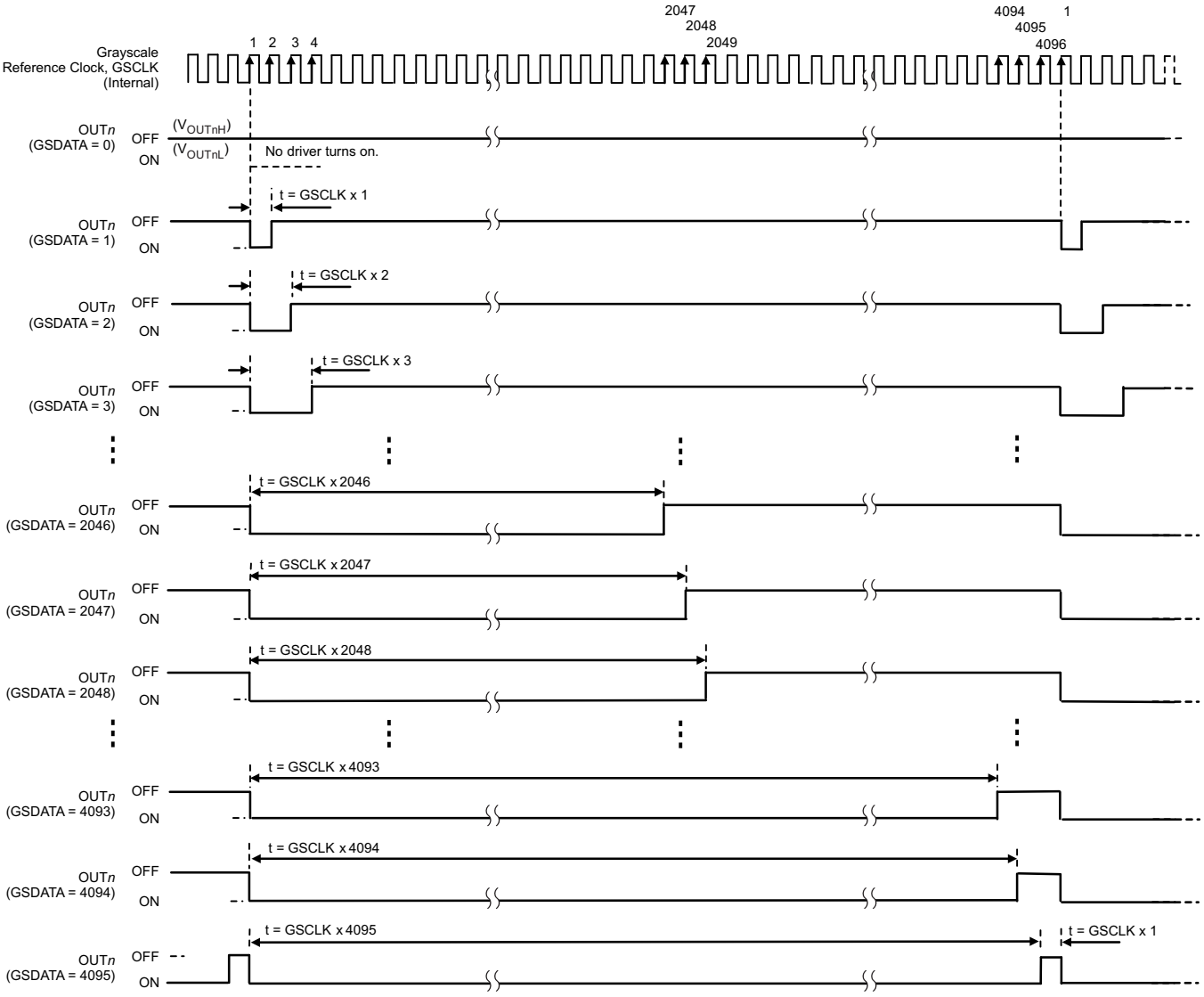
Table 3 summarizes the GS data values versus the output ideal on-time duty cycle. Furthermore, actual on-time differs from the ideal on-time because the output drivers and control circuit have some timing delay. When the device is powered on, all outputs are forced off and remain off until the non-zero GS data are written to the 36-bit GS data latch.

Table 3. Output Duty Cycle and Total On-Time versus GS Data

GS DATA		NO. OF GSCLKs OUT*n* TURNS ON	NO. OF GSCLKs OUT*n* TURNS OFF	TOTAL IDEAL TIME (µs)	ON-TIME DUTY (%)
DECIMAL	HEX				
0	0	Off	Off	0	0
1	1	1	2	0.08	0.02
2	2	1	3	0.17	0.05
—	—	—	—	—	—
255	0FE	1	256	21.25	6.23
256	0FF	1	257	21.33	6.25
257	100	1	258	21.42	6.27
—	—	—	—	—	—
511	1FF	1	512	42.58	12.48
512	200	1	513	42.67	12.50
513	201	1	514	42.75	12.52
—	—	—	—	—	—
1023	3FF	1	1024	85.25	24.98
1024	400	1	1025	85.33	25.00
1025	401	1	1026	85.42	25.00
—	—	—	—	—	—
2047	7FF	1	2048	170.6	49.98
2048	800	1	2049	170.7	50.00
2049	801	1	2050	170.8	50.02
—	—	—	—	—	—
4093	FFD	1	4094	341.1	99.93
4094	FFE	1	4095	341.2	99.95
4095	FFF	1	4096	341.3	99.98

PWM Control

The GS counter keeps track of the number of grayscale reference clocks (GSCLKs) from the internal oscillator. Each output stays on while the counter is less than or equal to the programmed GS value. Each output turns off when the GS counter is greater than the GS value in the 36-bit GS data latch. Figure 16 illustrates the PWM operation timing.



(1) Actual on-time differs from the ideal on-time.

Figure 16. PWM Operation

REGISTER AND DATA LATCH CONFIGURATION

The TLC5973 has a 48-bit shift register and a 36-bit data latch that stores GS data. When the internal GS data latch pulse is generated and the data of the 12 MSBs in the shift register are 3AAh, the lower 36-bit data in the 48-bit shift register are copied into the 36-bit GS data latch. If the data of the eight MSBs is not 3AAh, the 36-bit data are not copied into the 36-bit GS data latch. Figure 17 shows the shift register and GS data latch configurations. Table 4 shows the 48-bit shift register bit assignment.

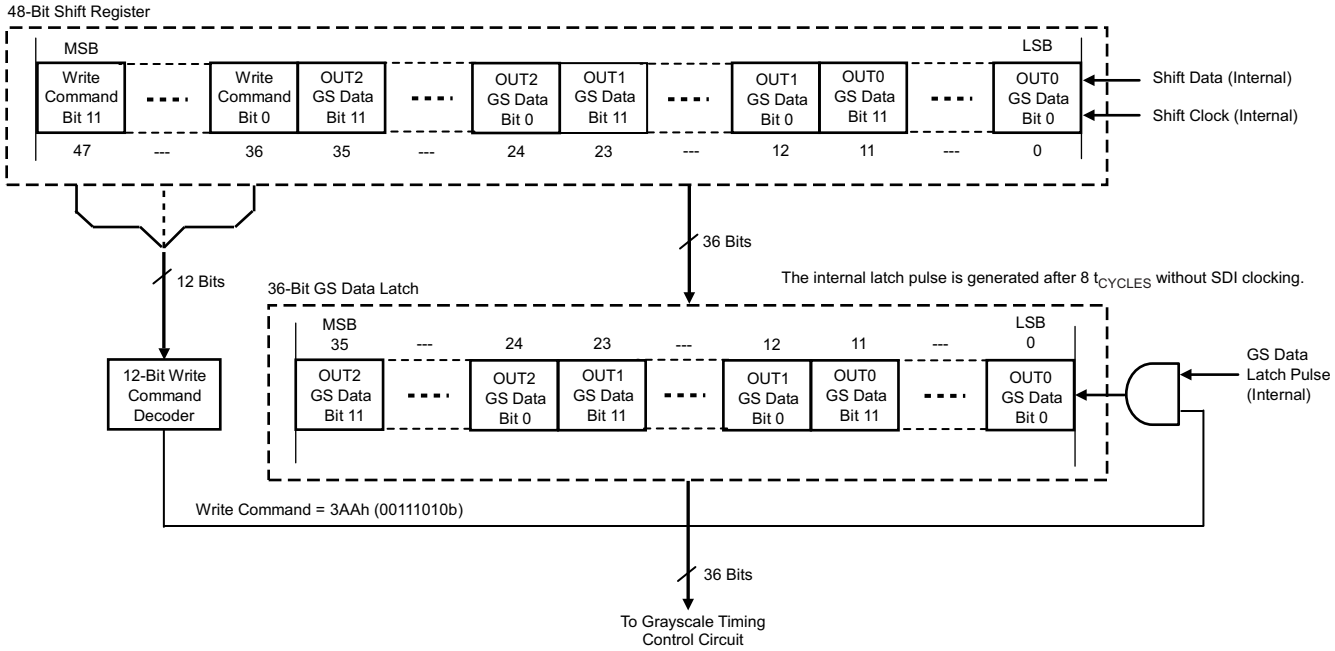


Figure 17. Common Shift Register and Control Data Latches Configuration

Table 4. 48-Bit Shift Register Data Bit Assignment

BITS	BIT NAME	CONTROLLED CHANNEL/FUNCTIONS
0 to 11	GSOUT0	GS data bits 0 to 11 for OUT0
12 to 23	GSOUT1	GS data bits 0 to 11 for OUT1
24 to 35	GSOUT2	GS data bits 0 to 11 for OUT2
36 to 47	WRTCMD	Data write command (3AAh) for GS data. The lower 36-bit GS data in the 48-bit shift register are copied to the GS data latch when the internal GS latch is generated (when these data bits are 3AAh, *001110101010b*).

ONE-WIRE INTERFACE (EasySet) DATA WRITING METHOD

There are four sequences to write GS data into the TLC5973 via a single-wire interface. This section discusses each sequence in detail.

Data Transfer Rate (t_{CYCLE}) Measurement Sequence

The TLC5973 measures the time between the first and second SDI rising edges either after the device is powered up or when the GS data latch sequence is executed (as described in the *GS Data Latch Sequence (GSLAT)* section) and the time is internally stored as t_{CYCLE}. t_{CYCLE} serves as a base time used to recognize one complete data write operation, a 48-bit data write operation, and a GS data write operation to the GS data latch. t_{CYCLE} can be set between 0.2 µs and 10 µs ($f_{CLK(SDI)}$ = 100 kHz to 3000 kHz). In this sequence, two instances of data '0' are written to the LSB side of the 48-bit shift register. Figure 18 shows the t_{CYCLE} measurement timing.

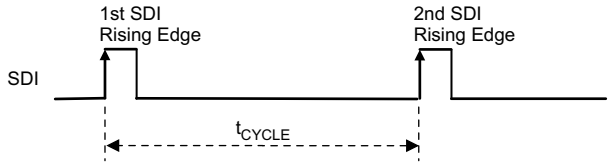


Figure 18. Data Transfer Rate (t_{CYCLE}) Measurement

Data '0' and Data '1' Write Sequence (Data Write Sequence)

When the second SDI rising edge is not input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the second rising edge is recognized as data '0'. When the second SDI rising edge is input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the second rising edge is recognized as data '1'. This write sequence must be repeated 46 times after the t_{CYCLE} measurement sequence in order to send the write command to the lower 10-bit (3AAh) and 48-bit GS data. Figure 19 shows the data '0' and '1' write timing.

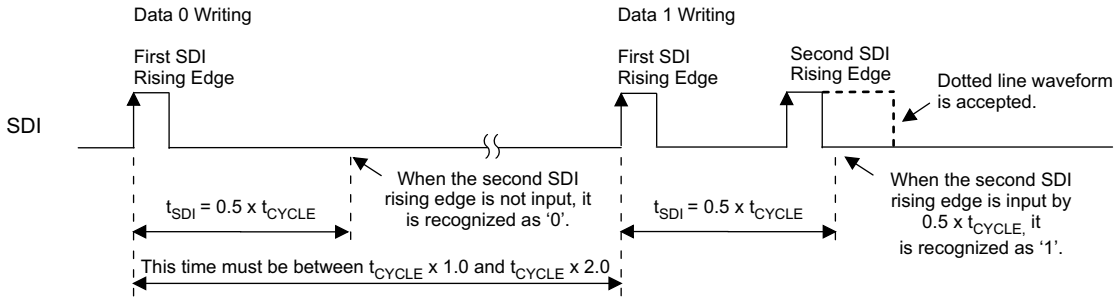


Figure 19. Data '0' and '1' Write Operation

One Communication Cycle End of Sequence (EOS)

One communication cycle end of sequence (EOS) must be input after the 48-bit data are written because the TLC5973 does not count the number of input data. When SDI is held low for the EOS hold time (t_{H0}), the 48-bit shift register values are locked and a buffered SDI signal is output from SDO to transfer GS data to the next device. Figure 20 shows the EOS timing.

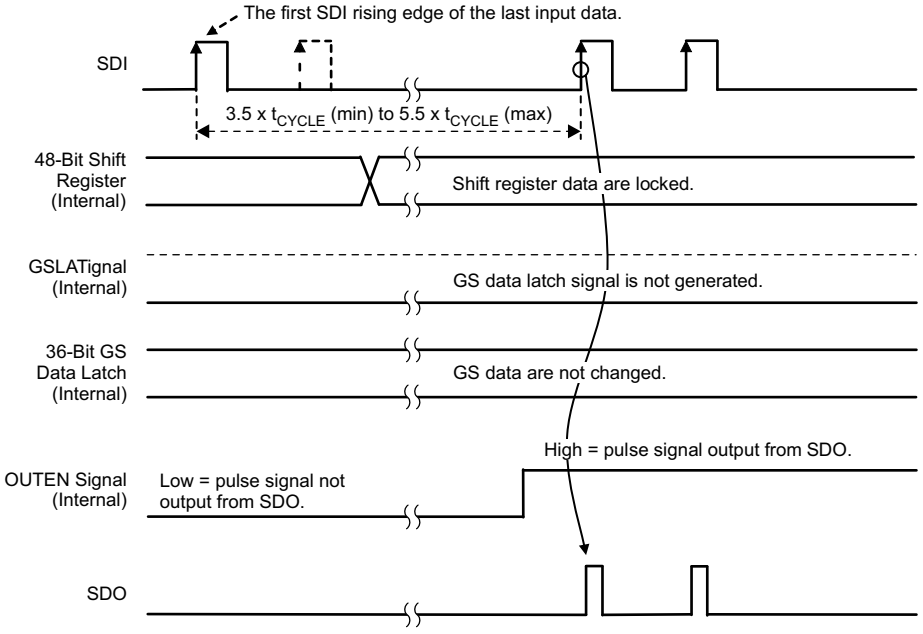


Figure 20. End of Sequence (EOS)

GS Data Latch (GSLAT) Sequence

A GS data latch (GSLAT) sequence must be input after the 48-bit data for all cascaded devices are written. When SDI is held low for the data latch hold time (t_{H1}), the 48-bit shift register data in all devices are copied to the GS data latch in each device. Furthermore, PWM control starts with the new GS data at the same time. Figure 21 shows the GSLAT timing.

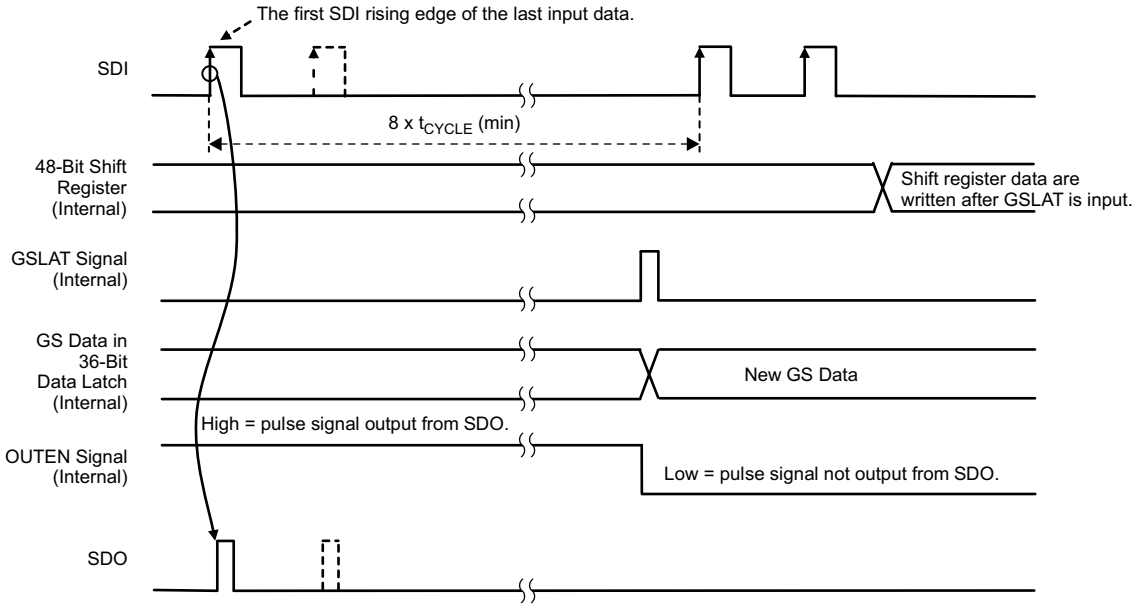


Figure 21. GS Data Latch Sequence (GSLAT)

HOW TO CONTROL DEVICES CONNECTED IN SERIES

The 12-bit write command and 36-bit grayscale (GS) data for OUT0 to OUT2 (for a total of 48 bits of data) must be written to the device.Figure 22 shows the 48-bit data packet configuration. When multiple devices are cascaded (as shown in Figure 23), *N* times the packet must be written into each TLC5973 in order to control all devices. There is no limit on how many devices can be cascaded, as long as proper VCC voltage is supplied. The packet for all devices must be written again whenever any GS data changes.

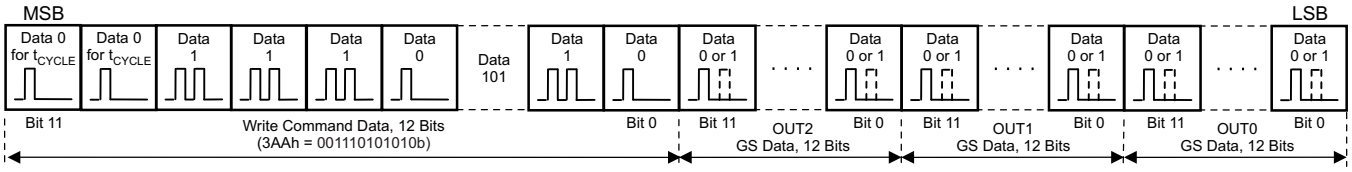


Figure 22. 48-Bit Data Packet Configuration for One TLC5973

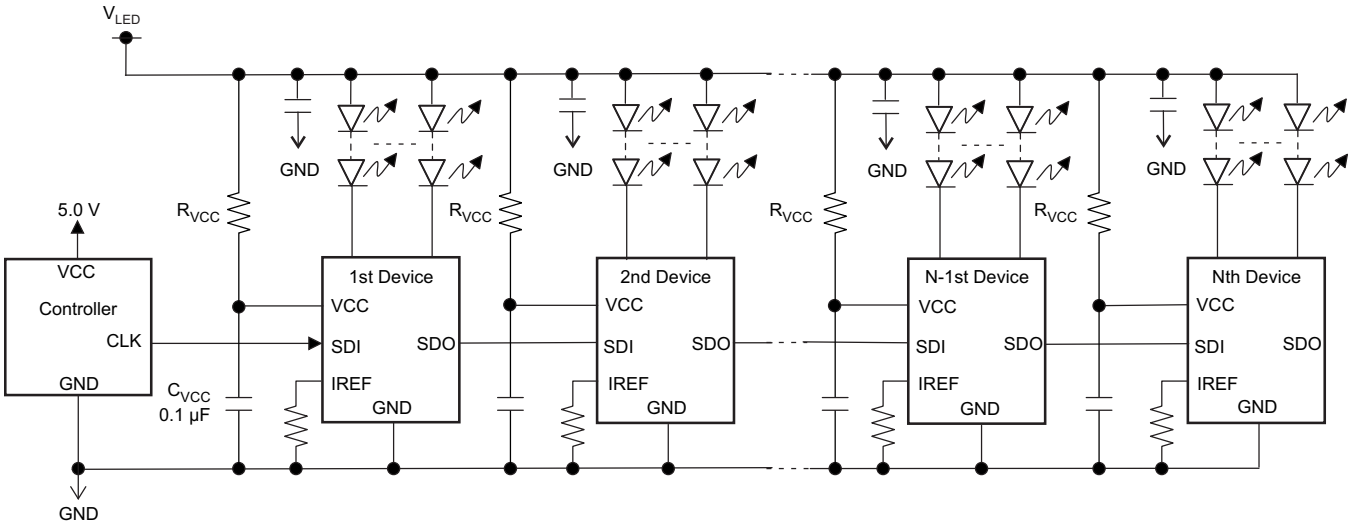


Figure 23. Cascade Connection of *N* TLC5973 Units (Internal Shunt Regulator Mode)

Refer to Figure 24 for the 48-bit data packet, EOS, and GSLAT input timing of all devices. The function setting write procedure and display control is as follows:

1. Power-up VCC (V_{LED}); all OUT*n* are off because GS data are not written yet.
2. Write the 48-bit data packet (MSB-first) for the first device using t_{CYCLE} and the data write sequences illustrated in Figure 18 and Figure 19. The first 12 bits of the 48-bit data packet are used as the write command. The write command must be 3AAh (001110101010b); otherwise, the 36-bit GS data in the 48-bit shift register are not copied to the 36-bit GS data latch.
3. Execute one communication cycle EOS (refer to Figure 20) for the first device.
4. Write the 48-bit data packet for the second TLC5973 as described step 2. However, t_{CYCLE} should be set to the same timing as the first device.
5. Execute one communication cycle EOS for the second device.
6. Repeat steps 4 and 5 until all devices have GS data.
7. The number of total bits is 48 × *N*. After all data are written, execute a GSLAT sequence as described in Figure 21 in order to copy the 36-bit LSBs in the 48-bit shift resister to the 36-bit GS data latch in each device; PWM control starts with the written GS data at the same time.

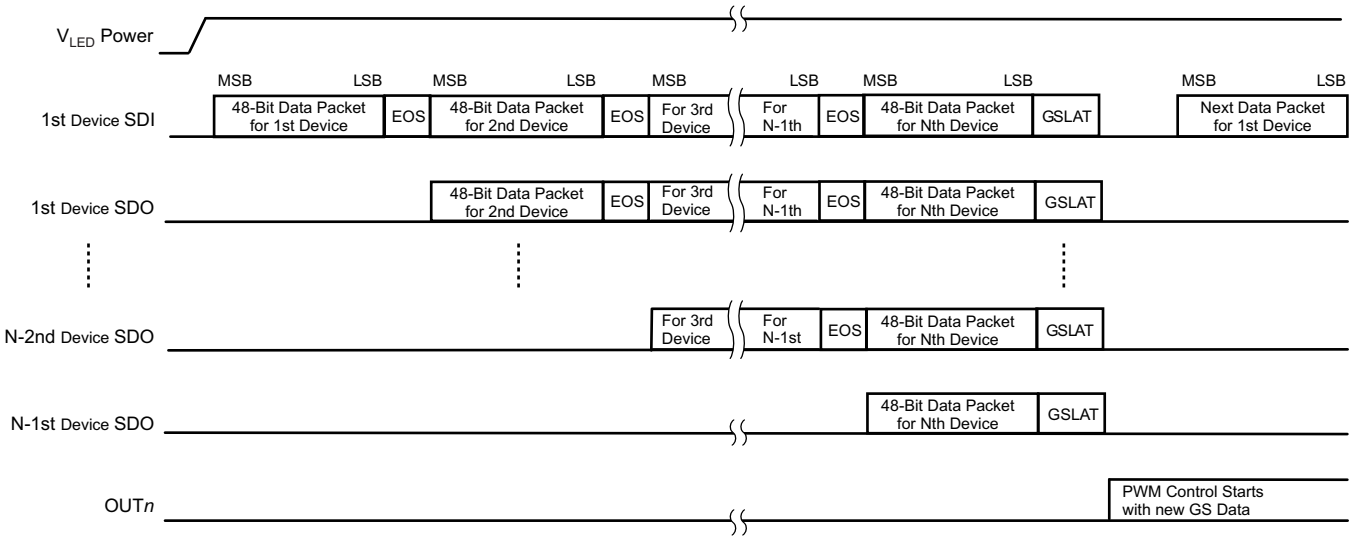


Figure 24. Data Packet Input Order for *N* TLC5973 Units

CONNECTOR DESIGN APPLICATION

When the connector pin of the device application printed circuit board (PCB) is connected or disconnected to other PCBs, the power must be turned off to avoid device malfunction or failure. Furthermore, designing the connector GND pin to be longer than other pins (as shown in Figure 25) is preferable. This arrangement allows the GND line to either be connected first or disconnected last, which is imperative for proper device function.

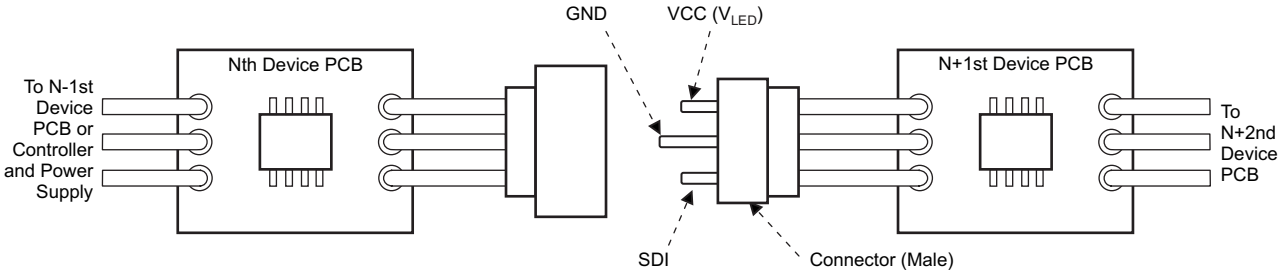


Figure 25. Connector Pin Design Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC5973D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5973	
TLC5973DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5973	

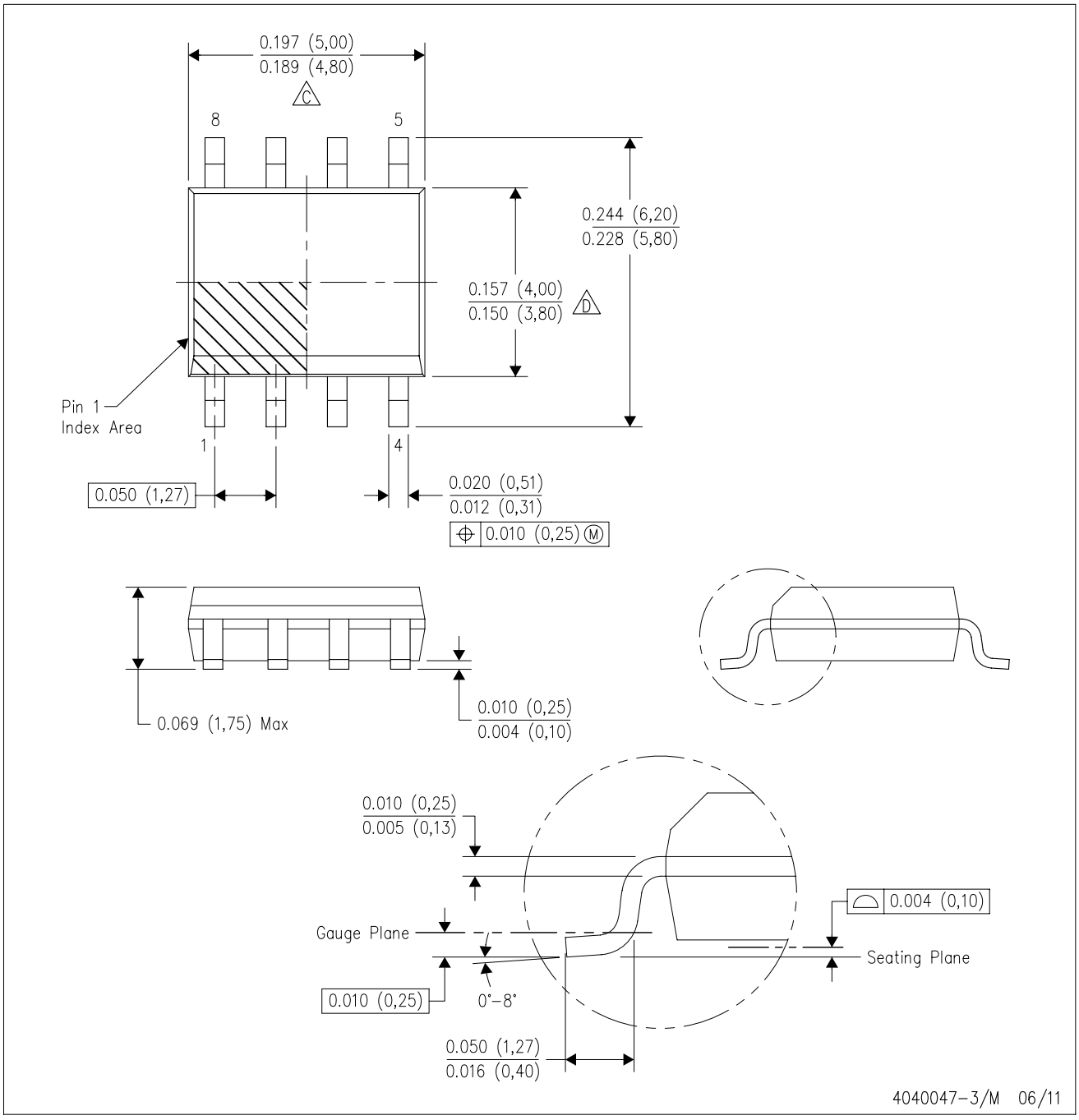
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

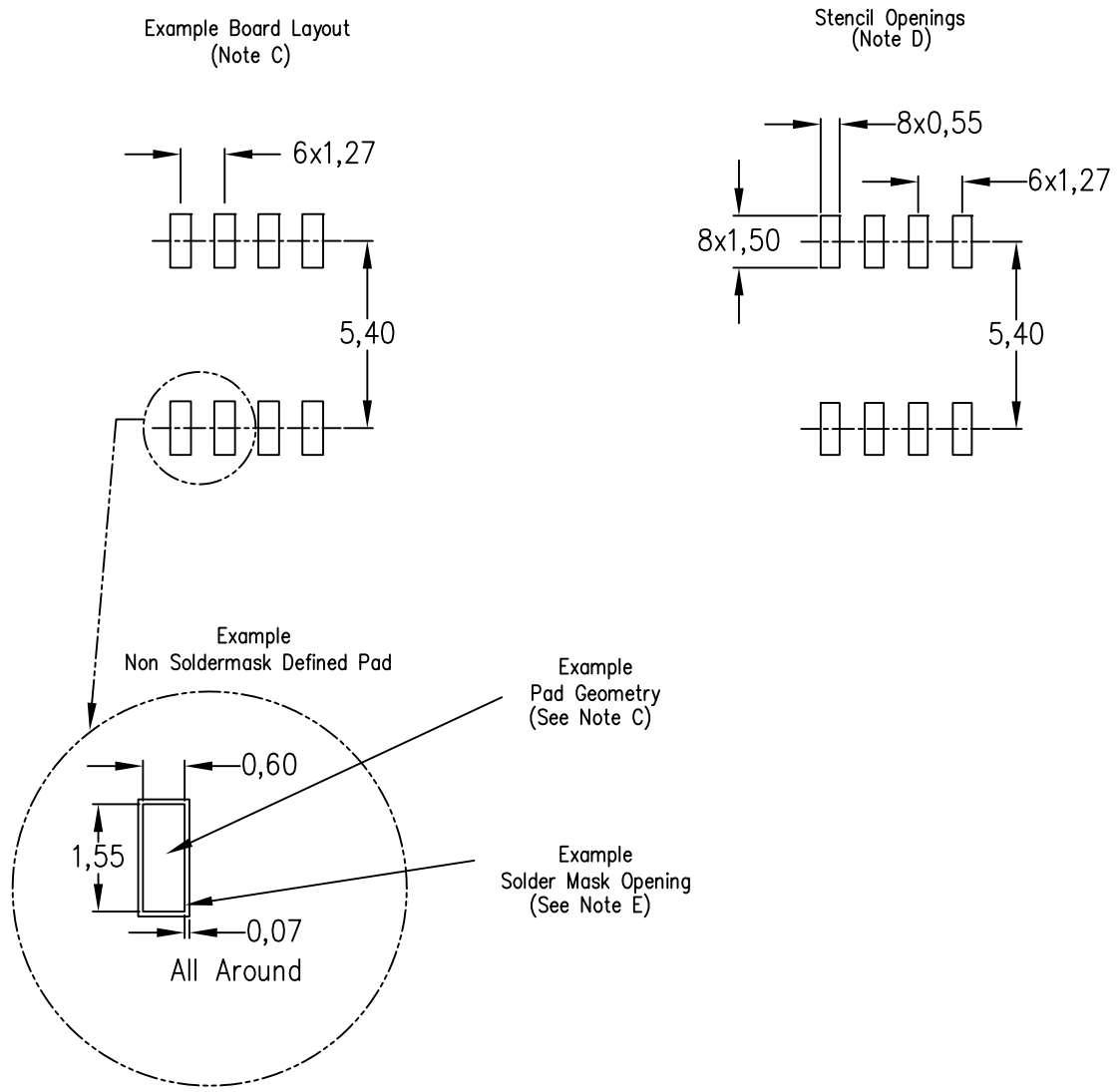
(4) Only one of markings shown within the brackets will appear on the physical device.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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