

FEATURES

- Excellent Temperature Stability
- Initial Tolerance...0.2% Max
- Dynamic Impedance...0.6 Ω Max
- Wide Operating Current Range
- Directly Interchangeable With LM136
- Needs No Adjustment for Minimum Temperature Coefficient

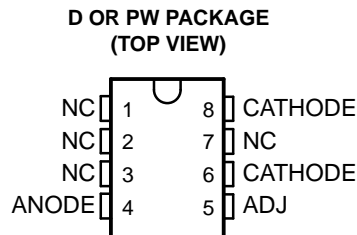
DESCRIPTION/ORDERING INFORMATION

The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. The maximum initial tolerance is ± 5 mV in the LP package and ± 10 mV in the D package. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient, α_{VZ} .

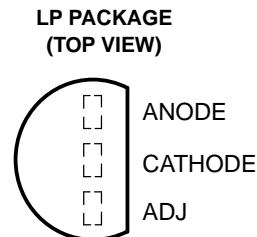
Although the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted $\pm 5\%$ to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

The LT1009 uses include 5-V system references, 8-bit analog-to-digital converter (ADC) and digital-to-analog converter (DAC) references, and power-supply monitors. The device also can be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from -40°C to 85°C.



NC – No internal connection



ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube of 75	LT1009CD	1009C
		Reel of 2500	LT1009CDR	
	TO-226/TO-92 – LP	Bulk of 1000	LT1009CLP	LT1009C
		Ammo of 2000	LT1009CLPM	
		Reel of 2000	LT1009CLPR	
	TSSOP – PW	Tube of 150	LT1009CPW	1009C
Reel of 2000		LT1009CPWR		
-40°C to 85°C	SOIC – D	Tube of 75	LT1009ID	1009I
		Reel of 2500	LT1009IDR	
	TO-226/TO-92 – LP	Bulk of 1000	LT1009ILP	LT1009I
		Ammo of 2000	LT1009ILPM	
		Reel of 2000	LT1009ILPR	
	TSSOP – PW	Tube of 150	LT1009IPW	1009I
		Reel of 2000	LT1009IPWR	

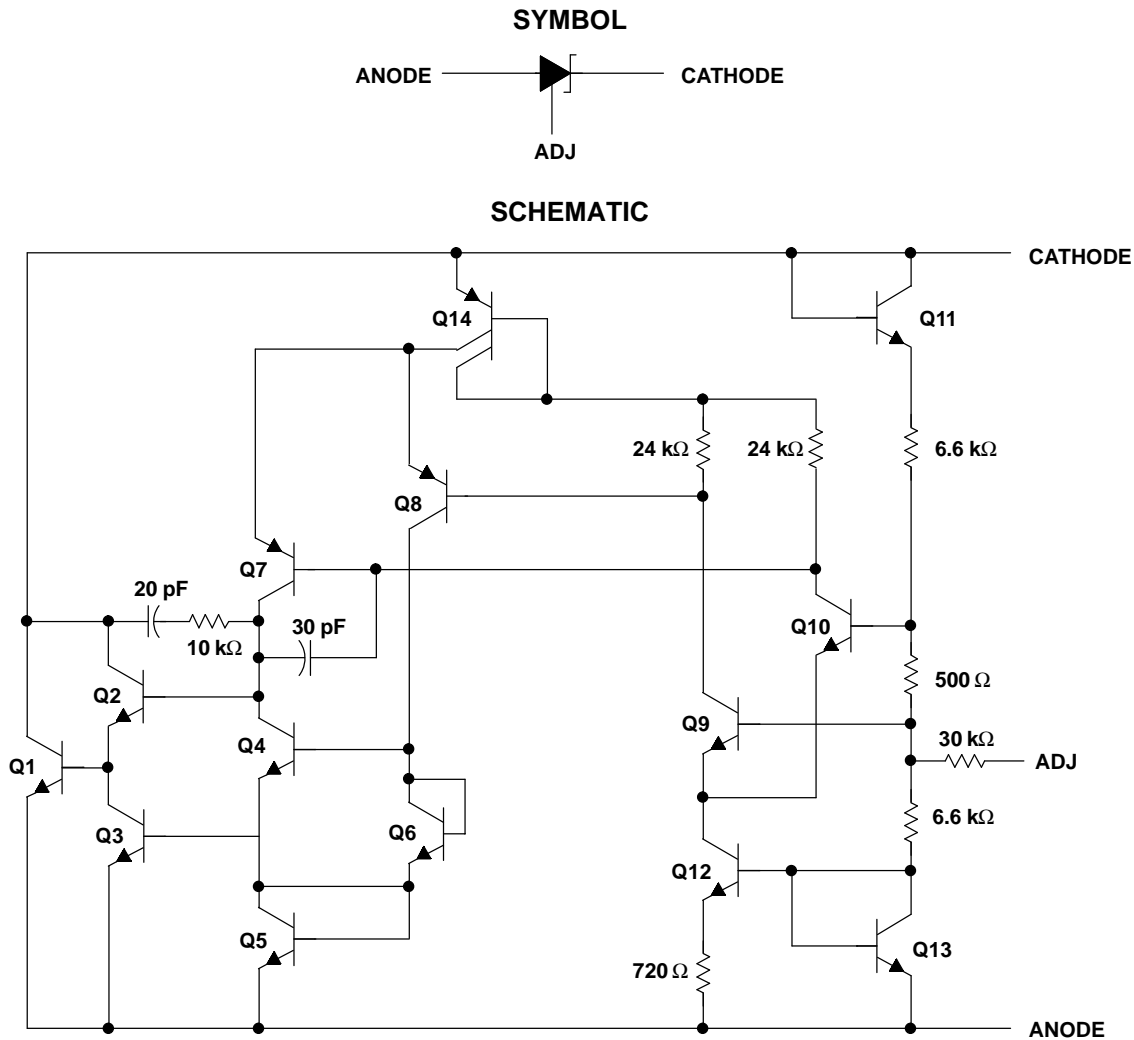
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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LT1009 2.5-V INTEGRATED REFERENCE CIRCUIT

SLVS013L–MAY 1987–REVISED SEPTEMBER 2005



NOTE: All component values shown are nominal.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_R	Reverse current		20	mA
I_F	Forward current		10	mA
θ_{JA}	Package thermal impedance ⁽²⁾⁽³⁾		97	°C/W
		D package		
		LP package	140	
	PW package		149	
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
T_A	Operating free-air temperature range	LT1009C	0	70	°C
		LT1009I	–40	85	

Electrical Characteristics

at specified free-air temperature

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	LT1009C			LT1009I			UNIT		
			MIN	TYP	MAX	MIN	TYP	MAX			
V_Z	Reference voltage	$I_Z = 1\text{ mA}$	D package	25°C	2.49	2.5	2.51	2.49	2.5	2.51	V
			LP package		2.495	2.5	2.505	2.495	2.5	2.505	
		Full range	D package	2.485		2.515	2.475		2.525		
			LP package	2.491		2.509	2.48		2.52		
V_F	Forward voltage	$I_F = 2\text{ mA}$	25°C	0.4		1	0.4		1	V	
	Adjustment range	$I_Z = 1\text{ mA}$, $V_{ADJ} = \text{GND to } V_Z$	25°C	125			125			mV	
		$I_Z = 1\text{ mA}$, $V_{ADJ} = 0.6\text{ V to } V_Z - 0.6\text{ V}$		45			45				
$\Delta V_{Z(\text{temp})}$	Change in reference voltage with temperature	D package	Full range	5			15			mV	
		LP package		4			15				
α_{V_Z}	Average temperature coefficient of reference voltage ⁽²⁾		0°C to 70°C	15			25			ppm/°C	
			–40°C to 85°C				20				35
ΔV_Z	Change in reference voltage with current	$I_Z = 400\text{ }\mu\text{A to } 10\text{ mA}$	25°C	2.6			10			mV	
			Full range				12				10
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	$I_Z = 1\text{ mA}$	25°C	20			20			ppm/khr	
Z_Z	Reference impedance	$I_Z = 1\text{ mA}$	25°C	0.3			1			Ω	
			Full range				1.4				1.4

(1) Full range is 0°C to 70°C for the LT1009C and –40°C to 85°C for the LT1009I.

(2) The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

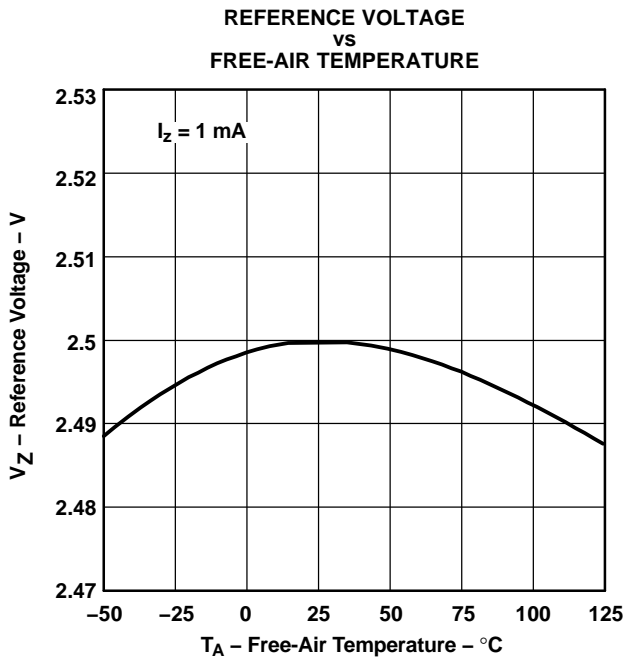


Figure 1.

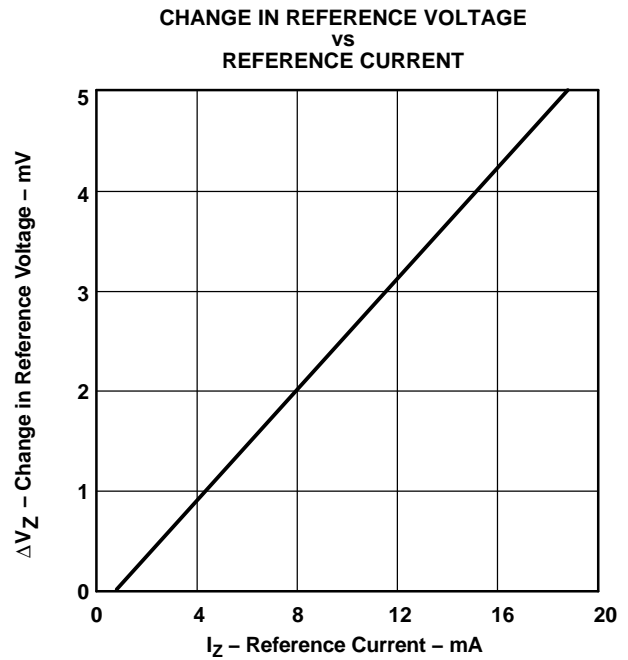


Figure 2.

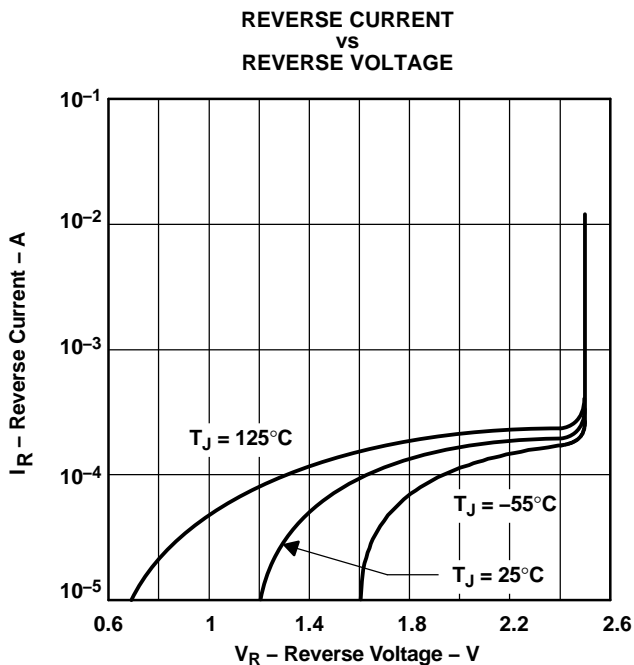


Figure 3.

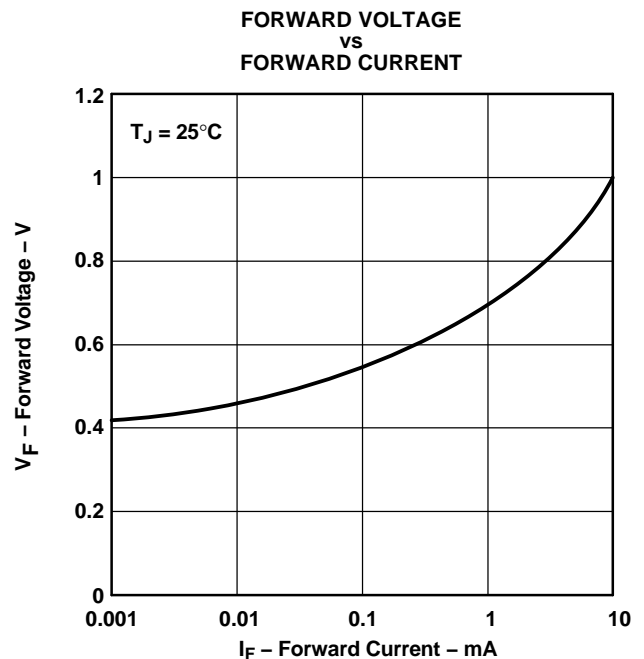


Figure 4.

TYPICAL CHARACTERISTICS (continued)

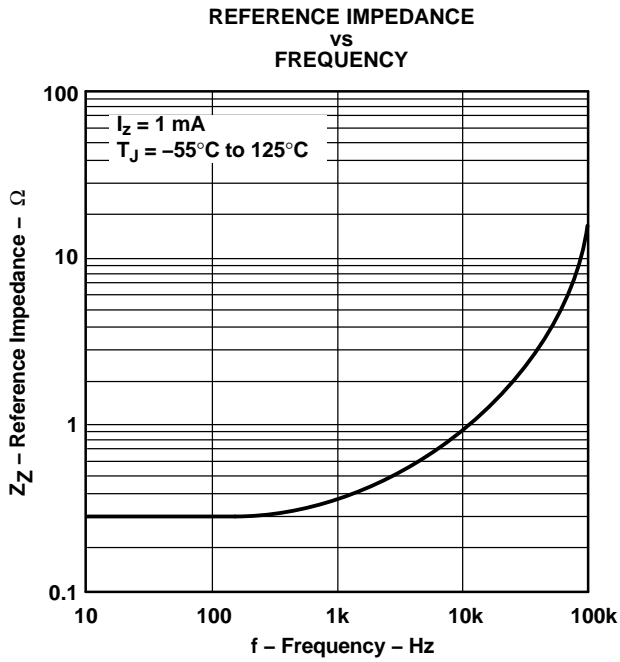


Figure 5.

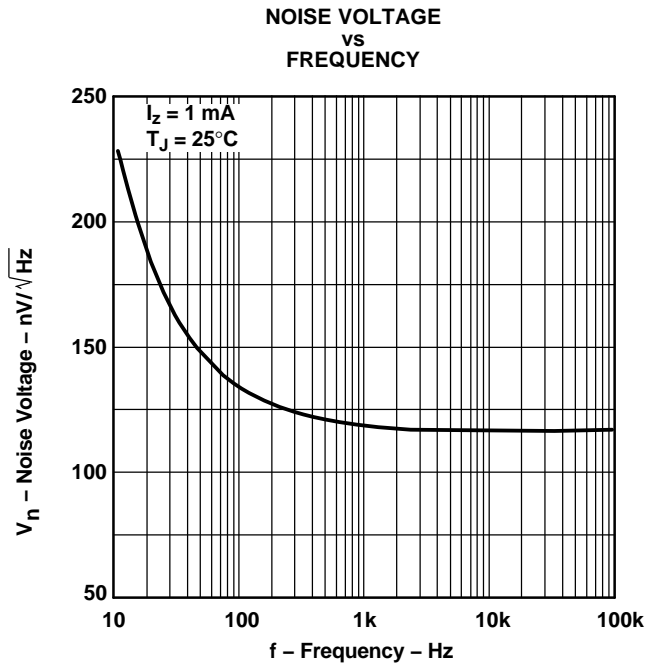


Figure 6.

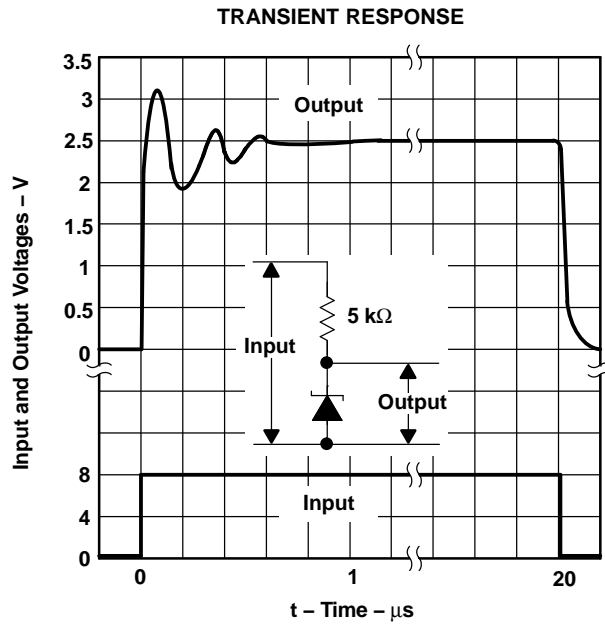
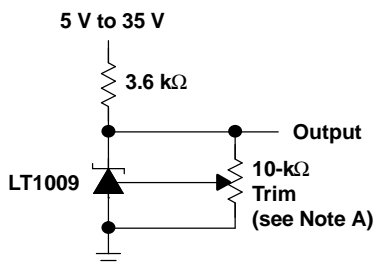


Figure 7.

APPLICATION INFORMATION



A. This does not affect temperature coefficient. It provides $\pm 5\%$ trim range.

Figure 8. 2.5-V Reference

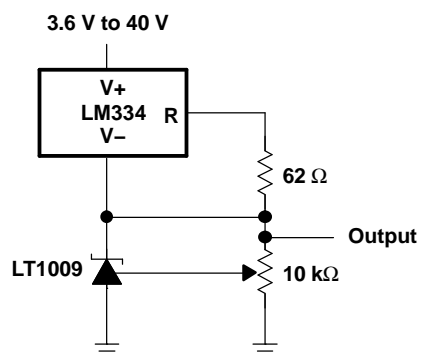


Figure 9. Adjustable Reference With Wide Supply Range

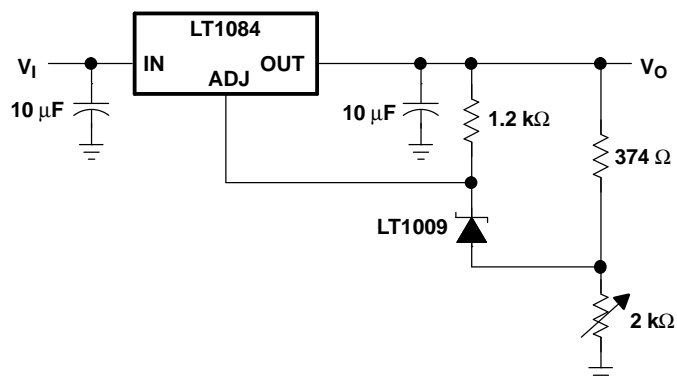


Figure 10. Power Regulator With Low Temperature Coefficient

APPLICATION INFORMATION (continued)

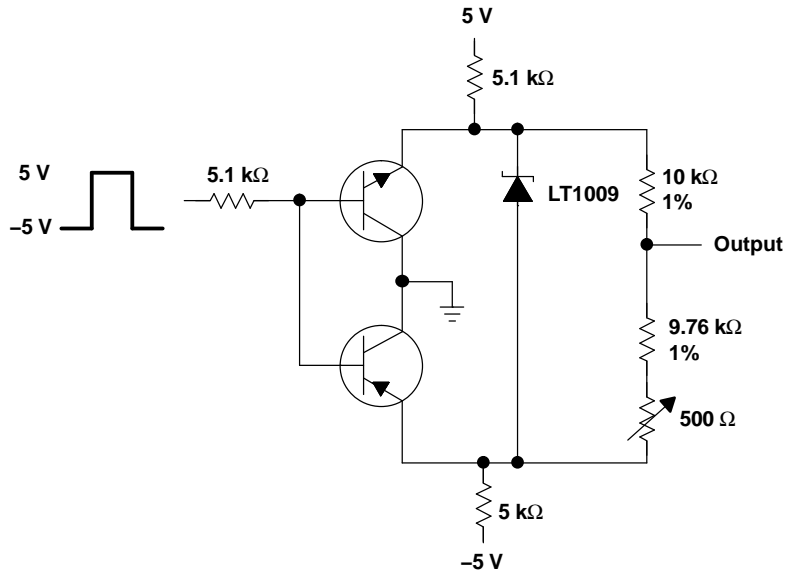


Figure 11. Switchable ±1.25-V Bipolar Reference

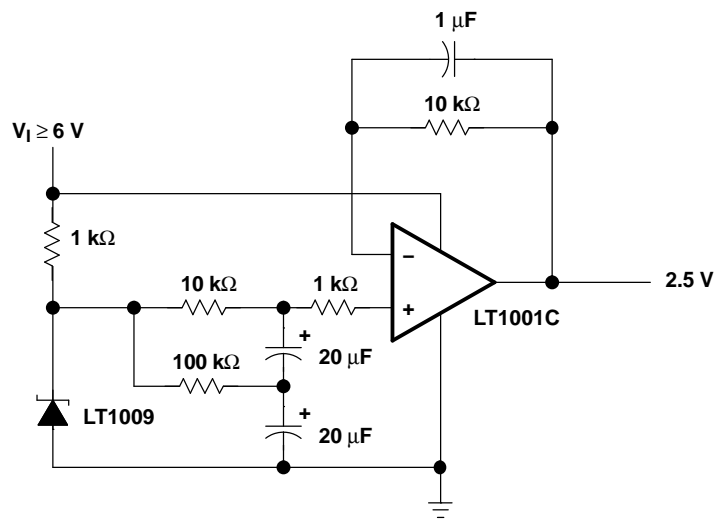


Figure 12. Low-Noise 2.5-V Buffered Reference

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
LT1009CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009CLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009CLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009CPK	OBSOLETE	SOT-89	PK	3		TBD	Call TI	Call TI
LT1009CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
LT1009ILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009ILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009ILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009ILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LT1009IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LT1009QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
LT1009Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1009CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1009CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LT1009IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1009IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1009CDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1009CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
LT1009IDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1009IPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G8)

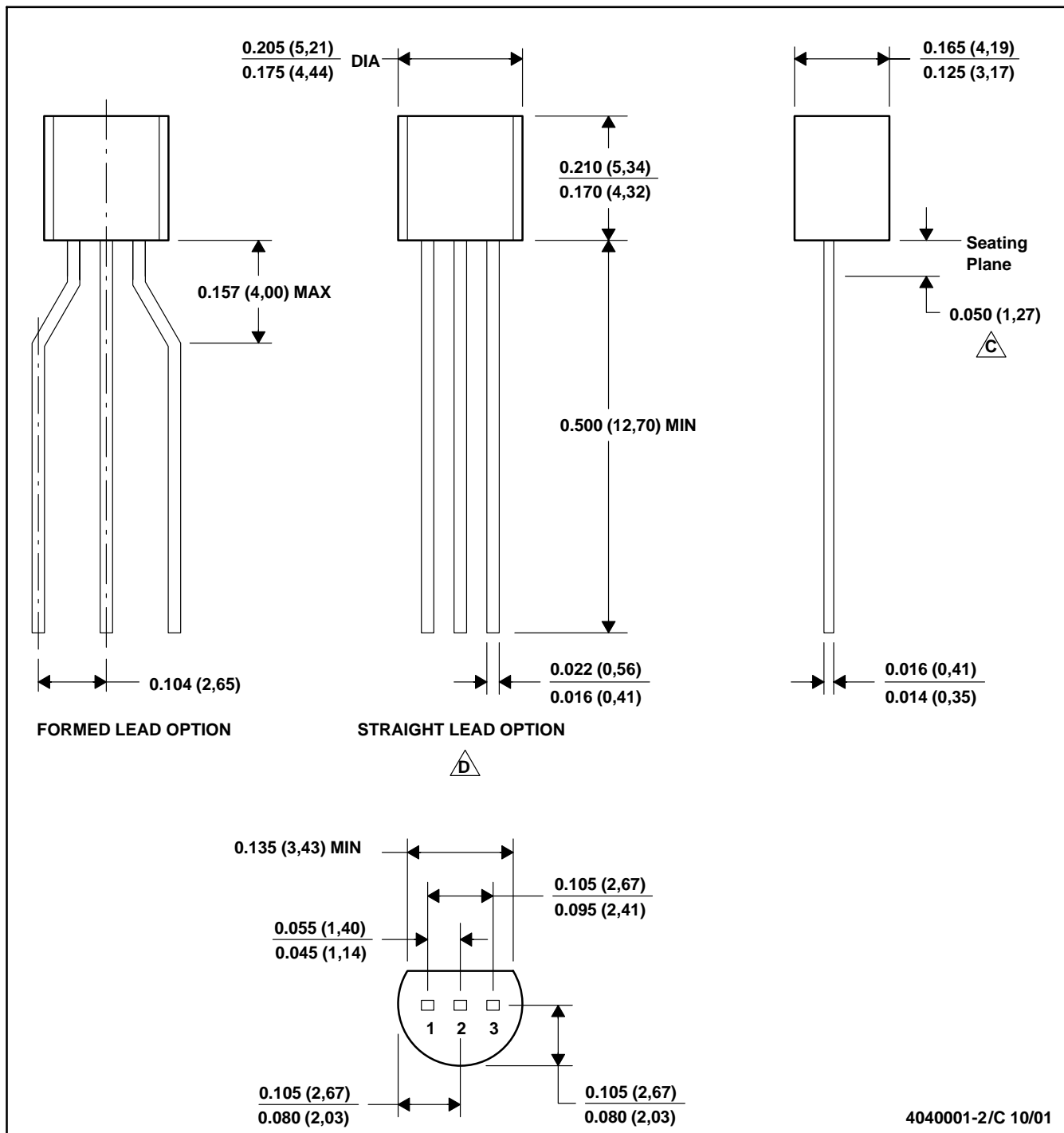
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



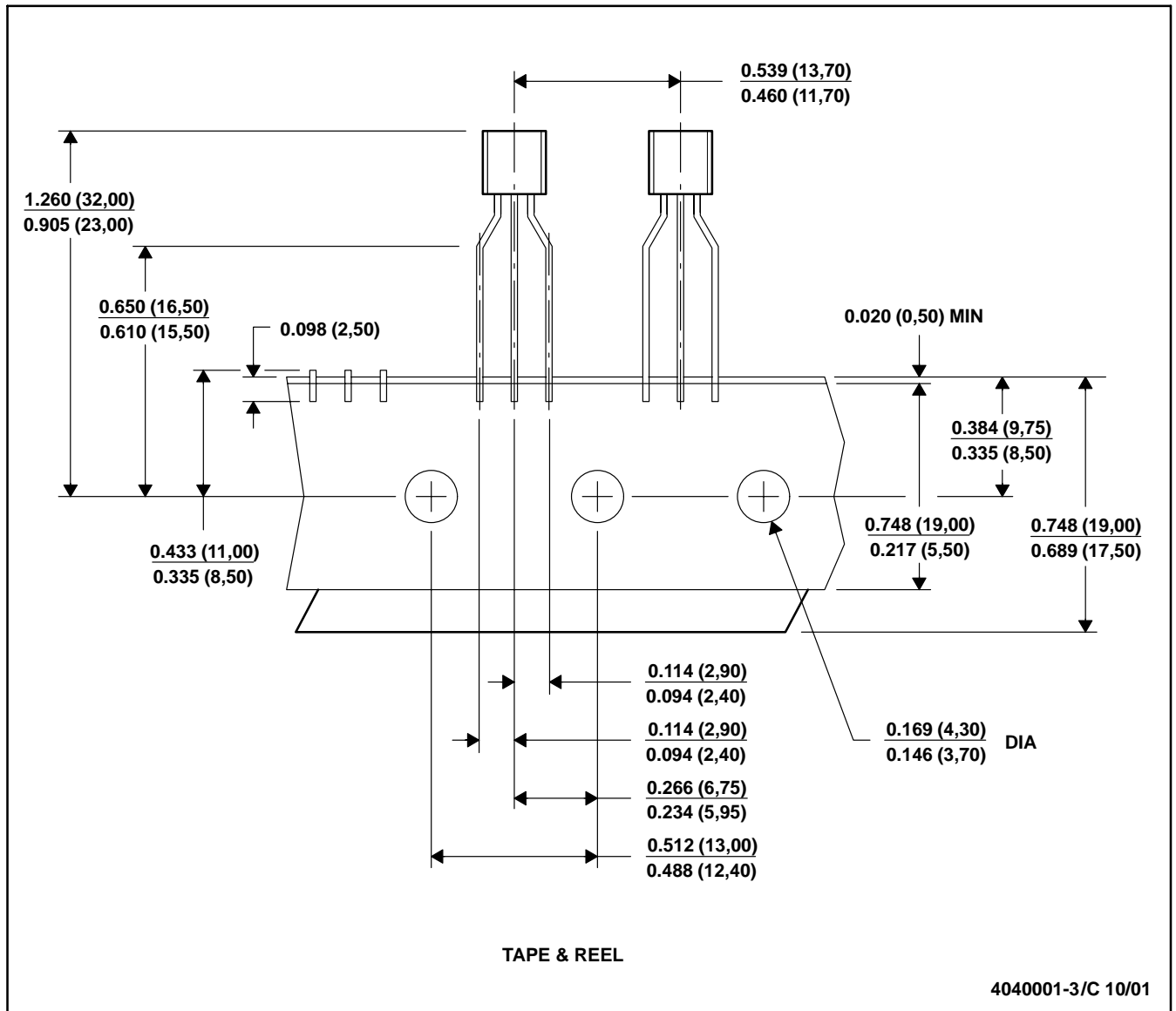
4040001-2/C 10/01

MECHANICAL DATA

MSOT002A – OCTOBER 1994 – REVISED NOVEMBER 2001

LP (O-PBCY-W3)

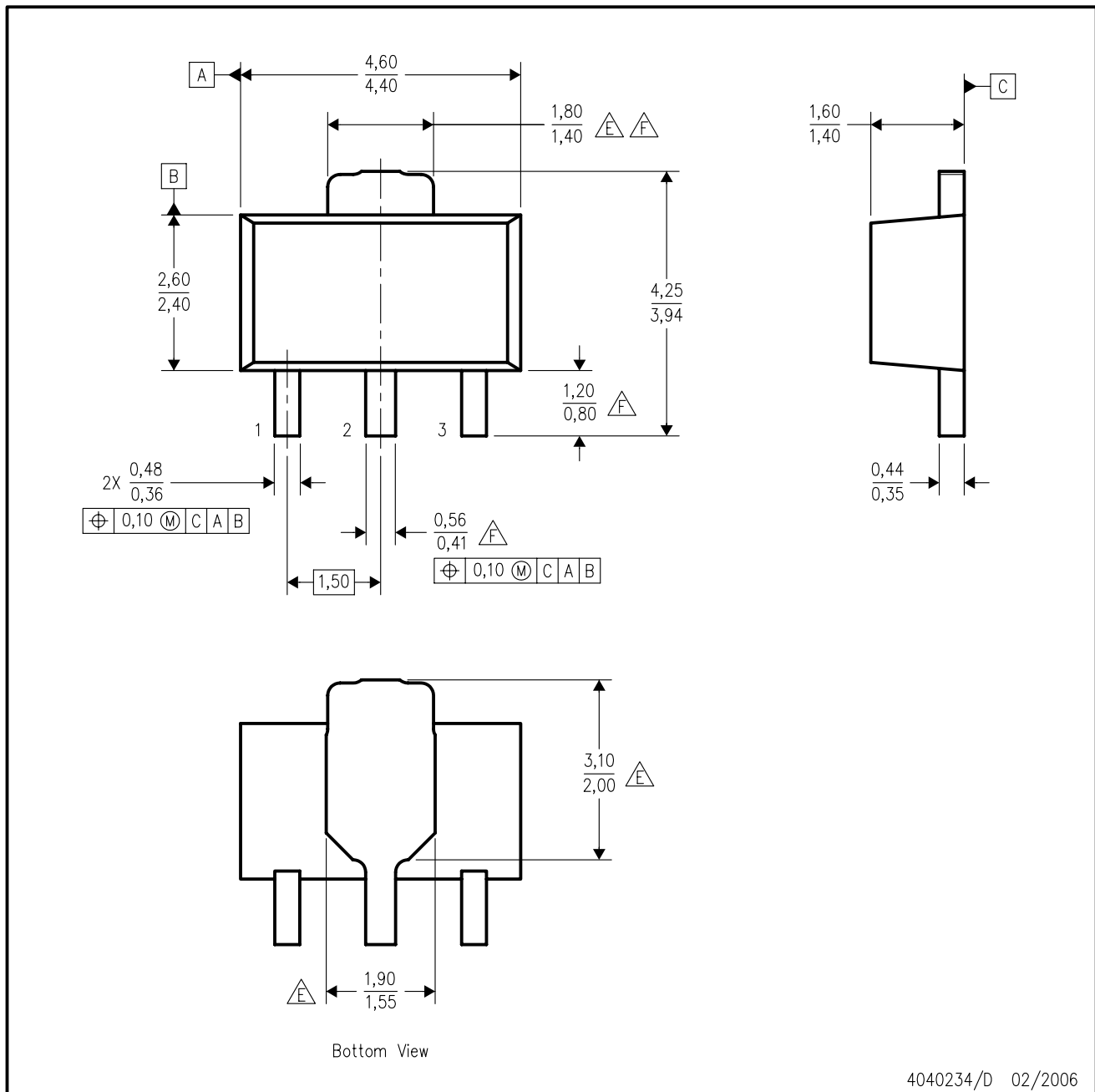
PLASTIC CYLINDRICAL PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Tape and Reel information for the Format Lead Option package.

PK (R-PSS0-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



4040234/D 02/2006

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - The center lead is in electrical contact with the tab.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- $\triangle E$ Thermal pad contour optional within these dimensions.
- $\triangle F$ Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

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